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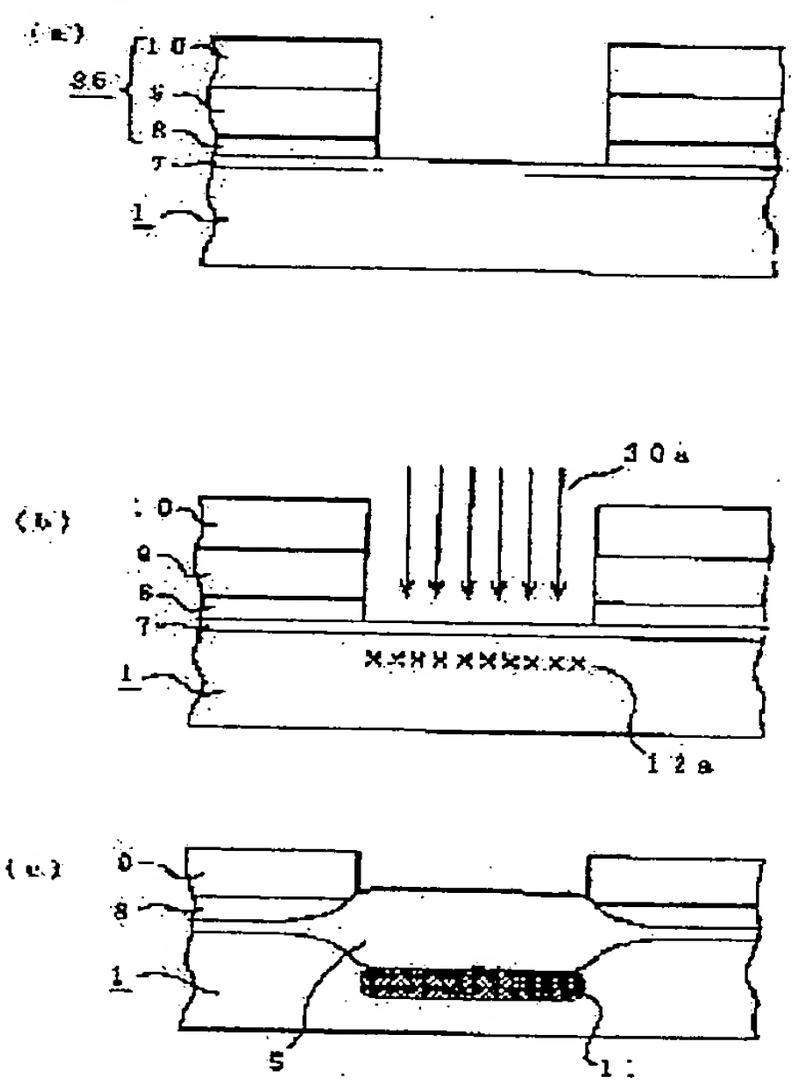
(54) SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a semiconductor device having a good isolation characteristic and low junction capacitance.
SOLUTION: On a Si substrate 1 having a silicon oxide film 7 on the surface a polycrystalline Si film 8, silicon nitride film 9 and resist 10 are laminated to form a mask 35. Using the mask 35, nitrogen ions 30a are implanted in the substrate 1 to form an N-implanted layer 12. The resist 10, a part of the mask 35, is removed, and using the resist-free mask, the substrate 1 is thermally oxidized to form a local oxidation of Si (LOCOS) isolation film 5 on the substrate surface and silicon nitride layer 11 is formed beneath this isolation film 5.



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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor device equipped with the component detached core formed in the above-mentioned silicon substrate surface of oxidation of the silicon substrate concerned using the mask formed on the front face of a silicon substrate, and the nitrogen content layer formed near the inferior surface of tongue of the above-mentioned component detached core of the ion implantation of the nitrogen to the above-mentioned silicon substrate using the above-mentioned mask.
[Claim 2] A nitrogen content layer is a semiconductor device according to claim 1 characterized by being the silicon nitride layer formed in the bottom of a component detached core.
[Claim 3] A nitrogen content layer is a semiconductor device according to claim 1 or 2 characterized by being formed in a configuration which encloses the inferior surface of tongue of a component detached core.
[Claim 4] A nitrogen content layer is a semiconductor device according to claim 1 characterized by being the nitriding silicon oxide layer formed in the interior of a component detached core.
[Claim 5] It has the component detached core formed in the semi-conductor substrate front face. The inside of the above-mentioned semi-conductor substrate front face, Are near [in which the component detached core concerned is formed] the part, and the field which extended the part in which the above-mentioned component detached core is not formed even inside the component detached core concerned is made into datum level. the semiconductor device characterized by thickness being about 1 law regardless of the width of face while the above-mentioned component detached core has two or more fields where the width of face in the vertical section to the above-mentioned datum level differs.
[Claim 6] It has the component detached core formed in the semi-conductor substrate front face. The inside of the above-mentioned semi-conductor substrate front face, Are near [in which the component detached core concerned is formed] the part, and the field which extended the part in which the above-mentioned component detached core is not formed even inside the component detached core concerned is made into datum level. the semiconductor device characterized by the thickness of the part above the above-mentioned datum level being about 1 law regardless of the width of face while the above-mentioned component detached core has two or more fields where the width of face in the vertical section to the above-mentioned datum level differs.
[Claim 7] While being formed in the field surrounded by the above-mentioned component detached core of the field in which the component detached core formed in the front face of a semi-conductor substrate and the component detached core of the above-mentioned semi-conductor substrate are formed It has the diffusion field in which the side face is in contact with the above-mentioned component detached core. The inside of the above-mentioned semi-conductor substrate front face, It is near [in which the component detached core concerned is formed] the part, and the field which extended the part in which the above-mentioned component detached core is not formed even inside the component detached core concerned is made into datum level. The above-mentioned component detached core the vertical section to this datum level -- setting -- the vertical section concerned -- the semiconductor device with

which the thickness of the part below the above-mentioned datum level to kick is about 1 law, and most side faces in which the above-mentioned diffusion field is in contact with the above-mentioned component detached core are characterized by being in contact with the component detached core concerned.

[Claim 8] The manufacture approach of a semiconductor device including the process which carries out the laminating of the polycrystalline-silicon film, a silicon nitride, and the resist to this order, and forms a mask on the silicon substrate by which silicon oxide was formed in the front face, the process which carry out the ion implantation of the nitrogen to the above-mentioned silicon substrate using the above-mentioned mask, the process which remove the resist which are some above-mentioned masks, and the process which oxidize the above-mentioned silicon substrate thermally using the mask from which the above-mentioned resist was removed.

[Claim 9] An ion implantation is the manufacture approach of the semiconductor device according to claim 8 characterized by being based on a slanting rotation ion implantation.

[Claim 10] The manufacture approach of a semiconductor device including the process which carries out the laminating of the polycrystalline silicon film and the silicon nitride to this order, and forms a mask at the silicon substrate top by which silicon oxide was formed in the front face, the process which oxidizes the above-mentioned silicon substrate thermally using the above-mentioned mask, and the process which carries out the ion implantation of the nitrogen to the above-mentioned silicon substrate using the above-mentioned mask.

[Claim 11] A mask is the manufacture approach of the semiconductor device according to claim 10 characterized by being formed in thickness which prevents that the nitrogen by which an ion implantation is carried out passes the mask concerned.

[Claim 12] The manufacture approach of a semiconductor device including the process which forms a mask on the front face of a semi-conductor substrate, the process which forms a component detached core by oxidizing thermally the above-mentioned semi-conductor substrate using the above-mentioned mask, and the process which carries out dry etching of the above-mentioned component detached core using the above-mentioned mask.

[Claim 13] The manufacture approach of a semiconductor device including the process which forms a mask on the front face of a semi-conductor substrate, the process which form a component detached core by oxidizing thermally the above-mentioned semi-conductor substrate using the above-mentioned mask, the process which form an insulator layer on the above-mentioned semi-conductor substrate, the process which carry out flattening of the above-mentioned insulator layer, the process which remove the insulator layer which carried out [above-mentioned] flattening until a part of upper limit of the above-mentioned mask is exposed, and the process which remove the above-mentioned mask.

[Claim 14] The manufacture approach of a semiconductor device including the process which carries out the laminating of the polycrystalline silicon film and the silicon nitride to this order, and forms a mask on the silicon substrate by which silicon oxide was formed in the front face, the process which carries out the slanting rotation ion implantation of the oxygen to the above-mentioned silicon substrate using the above-mentioned mask, and the process which oxidizes the above-mentioned silicon substrate thermally using the above-mentioned mask.

[Claim 15] The manufacture approach of a semiconductor device including the process which forms a component detached core in one principal plane of a silicon substrate, and the process which forms a channel cut field by carrying out the slanting rotation ion implantation of Lynn to one principal plane of the above-mentioned silicon substrate.

[Claim 16] The manufacture approach of a semiconductor device including the process which forms in one principal plane of a silicon substrate the component detached core which has a nitriding silicon oxide layer, and the process which forms a channel cut field by carrying out the slanting rotation ion implantation of the boron to one principal plane of the above-mentioned silicon substrate.

[Claim 17] The process which forms a channel cut field is the manufacture approach of the semiconductor device according to claim 15 or 16 characterized by including the process which re-diffuses poured-in Lynn or boron by annealing treatment.

[Claim 18] The manufacture approach of a semiconductor device including the process which carries out the laminating of the polycrystalline-silicon film and the silicon nitride to this order, and forms a mask at the silicon substrate top by which silicon oxide was formed in the front face, the process which oxidize the above-mentioned silicon substrate thermally using the above-mentioned mask, the process which form in the above-mentioned mask side face the sidewall which consists of a resist, the process which carry out an ion implantation inside the above-mentioned silicon substrate by using the above-mentioned sidewall as a mask, and the process which remove the above-mentioned sidewall by etching.
[Claim 19] On the silicon substrate by which silicon oxide was formed in the front face, the laminating of the polycrystalline silicon film and the silicon nitride is carried out to this order. The process which forms a mask, and the process which forms in the side face of the above-mentioned mask the sidewall which consists of a resist, The process which carries out an ion implantation to the interior of the above-mentioned silicon substrate by using the above-mentioned sidewall as a mask, The manufacture approach of a semiconductor device including the process which removes the above-mentioned sidewall by etching, and the process which oxidizes the above-mentioned silicon substrate thermally using the mask which consists of the above-mentioned polycrystalline silicon film and a silicon nitride.
[Claim 20] A sidewall is the manufacture approach of the semiconductor device according to claim 18 or 19 characterized by the selection ratio to etching forming according to the quality of the material higher than silicon oxide and a silicon nitride instead of a resist.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] It is related with LOCOS (LocalOxidation of Silicon) which is a technique for this invention to perform electric separation between two or more component formation fields especially about the structure and its manufacture approach of a semiconductor device.
[0002]
[Description of the Prior Art] Conventionally, LOCOS (Local Oxidation of Silicon) has been widely used as the formation approach of the separation oxide film used for the isolation of a semiconductor integrated circuit. However, when Above LOCOS was used with detailed-izing of a semiconductor device, it had become the factor which occupies the area of a component formation field in an excess, consequently resists integration of a semiconductor circuit because lateral oxidization progresses beyond the need and a BAZU beak occurs. Then, Poly-Si using the mask of the structure which sandwiched the polycrystalline silicon film between silicon oxide and a silicon nitride in order to control this BAZU beak length in recent years buffered LOCOS (hereafter referred to as PBL.) is used increasingly.
[0003] The structure of the semiconductor device equipped with the separation oxide film which used PBL below and was formed in the silicon substrate surface, and the impurity range formed in the silicon substrate using the conventional manufacture approach is explained using drawing 24 and drawing 25 .
[0004] Drawing 24 is the important section sectional view showing the structure of the conventional semiconductor device, and is set to drawing 24 . The well field where 1 was formed in the silicon substrate and 2 was formed in one principal plane of a silicon substrate 1, The channel cut field formed in the part with 3 [shallower than the above-mentioned well field 2 of the principal plane of a silicon substrate 1], The channel dope field where 4 was formed in the component formation field 6 near the front face of a silicon substrate 1, 5 is formed so that the perimeter of the component formation field 6 may be surrounded, it separates electrically each of two or more component formation fields 6, for example, is a separation oxide film (LOCOS demarcation membrane) which has about 4000A thickness.
[0005] Drawing 25 is the important section sectional view showing the manufacture approach of the conventional semiconductor device in order of a process. first, the thing oxidized in silicon substrate 1 front face as shown in drawing 25 (a) -- for example, the silicon oxide 7 of about 50-500A thickness -- forming -- this silicon oxide 7 top -- for example, polycrystalline silicon film 8a of about 100-1000A thickness and about 500-4000A thickness -- having -- a presentation -- Si3 N4 it is -- silicon nitride 9a is deposited on this order. Here, silicon oxide 7 may be formed with a CVD method.
[0006] Next, as shown in drawing 25 (b), while applying a resist on a silicon substrate 1 and carrying out patterning of the resist concerned using the usual photoengraving-process technique, using the resist 10 by which patterning was carried out, sequential etching of above-mentioned silicon nitride 9a and the polycrystalline silicon film 8a is carried out, and the mask which consists of the silicon nitride 9 and the polycrystalline silicon film 8 is formed. .
[0007] Next, as shown in drawing 25 (c), a resist 10 is removed, a silicon substrate 1 is oxidized

thermally using the mask which consists of polycrystalline silicon film 8 and a silicon nitride 9, and the separation oxide film 5 which is a LOCOS demarcation membrane is formed. Then, etching removes the polycrystalline silicon film 8 and the silicon nitride 9.
[0008] Next, as shown in drawing 25 (d), the ion implantation (well impregnation) of the impurity 27 for forming the well field 2 is performed, and impurity range 2a used as the well field 2 is formed in a silicon substrate 1. Here, although energy which is with the case of P type well formation and the case of N type well formation, and is different among the generations of a manufacture process, respectively is used for impregnation energy, specifically, the high energy of 100 - 2000keV extent is used for it.
[0009] Next, as shown in drawing 25 (e), the ion implantation (channel cut impregnation) of the impurity 28 for forming the channel cut field 3 is performed, and impurity range 3a used as the channel cut field 3 is formed. Here, specifically, the energy of 100 - 1000keV extent is used for impregnation energy. In order to separate electrically each of two or more component formation fields 6, this channel cut impregnation pours in the impurity of the same conductivity type as well impregnation so that impurity range 3a may be formed directly under the separation oxide film 5.
[0010] Next, as shown in drawing 25 (f), the ion implantation (channel dope impregnation) of the impurity 29 for forming the channel dope field 4 is performed, and impurity range 4a used as the channel dope field 4 is formed. Here, specifically, the energy of 5 - 100keV extent is used for impregnation energy. This channel dope impregnation is poured in near the front face of a silicon substrate 1, in order to control threshold electrical potential differences, such as an MOS transistor formed in the component formation field 6.
[0011] Then, the semiconductor device shown by drawing 24 is obtained through processes, such as annealing treatment.
[0012]
[Problem(s) to be Solved by the Invention] However, in the semiconductor memory carried out in this way, when there were few injection rates in channel cut impregnation, there was a problem that isolation will be impossible according to a punch through condenser etc. depending on the conditions of the bias concerning the source drain field formed in the component formation field 6. On the other hand, when the injection rate in this channel cut impregnation was made [many], there was also a problem that the junction capacitance of the channel cut field 3 and the source drain field formed in the component formation field 6 increased.
[0013] This invention is made in view of the above-mentioned point, and while the separation engine performance is good, it aims at offering the semiconductor device which a junction capacitance does not increase.
[0014]
[Means for Solving the Problem] The semiconductor device concerning this invention prepares the component detached core formed in the above-mentioned silicon substrate surface of oxidation of the silicon substrate concerned using the mask formed on the front face of a silicon substrate, and the nitrogen content layer formed near the underside of the above-mentioned component detached core of the ion implantation of the nitrogen to the above-mentioned silicon substrate using the above-mentioned mask.
[0015] Moreover, the above-mentioned nitrogen content layer is characterized by being the silicon nitride layer formed in the bottom of a component detached core.
[0016] Moreover, the above-mentioned nitrogen content layer is characterized by being formed in a configuration which encloses the underside of a component detached core.
[0017] Moreover, the above-mentioned nitrogen content layer is characterized by being the nitriding silicon oxide layer formed in the interior of a component detached core.
[0018] It has the component detached core formed in the semi-conductor substrate front face. Moreover, the inside of the above-mentioned semi-conductor substrate front face, Are near [in which the component detached core concerned is formed] the part, and the field which extended the part in which the above-mentioned component detached core is not formed even inside the component detached core concerned is made into datum level. while the above-mentioned component detached core has two or more fields where the width of face in the

vertical section to the above-mentioned datum level differs, regardless of the width of face, it is characterized by thickness being about 1 law.
[0019] It has the component detached core formed in the semi-conductor substrate front face. Moreover, the inside of the above-mentioned semi-conductor substrate front face, Are near [in which the component detached core concerned is formed] the part, and the field which extended the part in which the above-mentioned component detached core is not formed even inside the component detached core concerned is made into datum level. while the above-mentioned component detached core has two or more fields where the width of face in the vertical section to the above-mentioned datum level differs, regardless of the width of face, it is characterized by the thickness of the part above the above-mentioned datum level being about 1 law.
[0020] Moreover, while being formed in the field surrounded by the above-mentioned component detached core of the field in which the component detached core formed in the front face of a semi-conductor substrate and the component detached core of the above-mentioned semi-conductor substrate are formed It has the diffusion field in which the side face is in contact with the above-mentioned component detached core. The inside of the above-mentioned semi-conductor substrate front face, It is near [in which the component detached core concerned is formed] the part, and the field which extended the part in which the above-mentioned component detached core is not formed even inside the component detached core concerned is made into datum level. The above-mentioned component detached core the vertical section to this datum level -- setting -- the vertical section concerned -- the thickness of the part below the above-mentioned datum level to kick is about 1 law, and the above-mentioned diffusion field is characterized by most side faces which are in contact with the above-mentioned component detached core being in contact with the component detached core concerned.
[0021] The manufacture approach of the semiconductor device concerning this invention carries out the laminating of the polycrystalline-silicon film, a silicon nitride, and the resist to this order, and possesses the process which forms a mask, the process which carry out the ion implantation of the nitrogen to the above-mentioned silicon substrate using the above-mentioned mask, the process which remove the resist which are some above-mentioned masks, and the process which oxidize the above-mentioned silicon substrate thermally using the mask from which the above-mentioned resist removed on the silicon substrate by which silicon oxide was formed in a front face.
[0022] Moreover, the above-mentioned ion implantation is characterized by being based on a slanting revolution ion implantation.
[0023] Moreover, on the silicon substrate by which silicon oxide was formed in the front face, the laminating of the polycrystalline silicon film and the silicon nitride is carried out to this order, and the process which forms a mask, the process which oxidizes the above-mentioned silicon substrate thermally using the above-mentioned mask, and the process which carries out the ion implantation of the nitrogen to the above-mentioned silicon substrate using the above-mentioned mask are provided.
[0024] Moreover, the above-mentioned mask is characterized by being formed in thickness which prevents that the nitrogen by which an ion implantation is carried out passes the mask concerned.
[0025] Moreover, the process which forms a mask on the front face of a semi-conductor substrate, the process which forms a component detached core by oxidizing thermally the above-mentioned semi-conductor substrate using the above-mentioned mask, and the process which carries out dry etching of the above-mentioned component detached core using the above-mentioned mask are provided.
[0026] Moreover, the process which forms a mask on the front face of a semi-conductor substrate, the process which form a component detached core by oxidizing thermally the above-mentioned semi-conductor substrate using the above-mentioned mask, the process which form an insulator layer on the above-mentioned semi-conductor substrate, the process which carry out flattening of the above-mentioned insulator layer, the process which remove the insulator layer which carried out [above-mentioned] flattening until a part of upper bed of the above-

mentioned mask is exposed, and the process which remove the above-mentioned mask provide.
[0027] Moreover, on the silicon substrate by which silicon oxide was formed in the front face, the laminating of the polycrystalline silicon film and the silicon nitride is carried out to this order, and the process which forms a mask, the process which carries out the slanting revolution ion implantation of the oxygen to the above-mentioned silicon substrate using the above-mentioned mask, and the process which oxidizes the above-mentioned silicon substrate thermally using the above-mentioned mask are provided.
[0028] Moreover, the process which forms a component detached core in one principal plane of a silicon substrate, and the process which forms a channel cut field by carrying out the slanting revolution ion implantation of Lynn to one principal plane of the above-mentioned silicon substrate are provided.
[0029] Moreover, the process which forms in one principal plane of a silicon substrate the component detached core which has a nitriding silicon oxide layer, and the process which forms a channel cut field by carrying out the slanting revolution ion implantation of the boron to one principal plane of the above-mentioned silicon substrate are provided.
[0030] Moreover, the process which forms the above-mentioned channel cut field is characterized by including the process which re-diffuses poured-in Lynn or boron by annealing treatment.
[0031] Moreover, the laminating of the polycrystalline-silicon film and the silicon nitride carries out to this order on the silicon substrate by which silicon oxide was formed in the front face, and the process which carries out an ion implantation, and the process which remove the above-mentioned sidewall by etching provide inside the above-mentioned silicon substrate by using as a mask the process which forms a mask, the process which oxidizes the above-mentioned silicon substrate thermally using the above-mentioned mask, the process which forms in the above-mentioned mask side face the sidewall which consists of a resist, and the above-mentioned sidewall.
[0032] Moreover, the laminating of the polycrystalline silicon film and the silicon nitride is carried out to this order on the silicon substrate by which silicon oxide was formed in the front face. The process which forms a mask, and the process which forms in the side face of the above-mentioned mask the sidewall which consists of a resist, The process which carries out an ion implantation to the interior of the above-mentioned silicon substrate by using the above-mentioned sidewall as a mask, The process which removes the above-mentioned sidewall by etching, and the process which oxidizes the above-mentioned silicon substrate thermally using the mask which consists of the above-mentioned polycrystalline silicon film and a silicon nitride are provided.
[0033] Moreover, the above-mentioned sidewall is characterized by the selection ratio to etching forming according to construction material higher than silicon oxide and a silicon nitride instead of a resist.
[0034]
[Embodiment of the Invention]
The gestalt 1 of implementation of this invention is explained below to gestalt 1. of operation based on drawing 1 thru/or drawing 3 . Drawing 1 is the important section sectional view showing the gestalt 1 of operation of this invention, in drawing 1 , 1 is a silicon substrate, and 5 is a LOCOS demarcation membrane which is the component detached core formed in this silicon substrate 1 front face. 11 is the silicon nitride layer formed in the bottom of the underside concerned near the underside of this LOCOS demarcation membrane 5.
[0035] Below, the manufacture approach of the semiconductor device constituted in this way is explained using drawing 2 and drawing 3 . Drawing 2 R> 2 and drawing 3 are the important section sectional views showing the gestalt 1 of this operation in order of a process, respectively.
[0036] The manufacture approach of 1 of the semiconductor device shown in above-mentioned drawing 1 is shown in drawing 2 . First, as shown in drawing 2 (a), on the silicon substrate 1 by which silicon oxide 7 is formed in the front face, the laminating of the polycrystalline silicon film 8, the silicon nitride 9, and the resist 10 is carried out to this order, and a mask 35 is formed

using the usual photoengraving-process technique.
[0037] Next, as shown in drawing 2 (b), without removing a resist 10, using the above-mentioned mask 35, nitrogen ion 30a is injected into the above-mentioned silicon substrate 1, and nitrogen impregnation layer 12a is formed. Here, suppose that energy with which nitrogen impregnation layer 12a is formed in the bottom of the underside concerned near the underside of the LOCOS demarcation membrane 5 formed in a next process is used for impregnation of nitrogen ion 30a. Moreover, among the above-mentioned semi-conductor substrate front faces, when the mask 35 concerned serves as an obstruction, nitrogen ion 30a is not injected into the part covered with the mask 35 here.
[0038] Next, as shown in drawing 2 (c), the LOCOS demarcation membrane 5 is formed in the silicon substrate 1 above-mentioned front face by oxidizing thermally the above-mentioned silicon substrate 1 using the mask 35 from which the resist 10 which are some above-mentioned masks 35 was removed, and this resist 10 was removed. Then, etching removes the above-mentioned mask 35 and the semiconductor device which has the silicon nitride layer 11 under the underside concerned near the underside of the above-mentioned LOCOS demarcation membrane 5 and which is shown in drawing 1 is obtained.
[0039] According to the manufacture approach of the semiconductor device shown in above-mentioned drawing 2 , it is not necessary to establish anew the photoengraving-process process for the mask formation for nitrogen ion 30a impregnation. The sake, Since the above-mentioned nitrogen ion 30a is poured in before being able to reduce the number of production processes of the semiconductor device shown in drawing 1 and performing thermal oxidation for formation of the LOCOS demarcation membrane 5 moreover Compared with the case where nitrogen ion is poured in, the nitrogen ion implantation equipment of high energy is not needed after formation of the LOCOS demarcation membrane 5, but it becomes possible to reduce the manufacturing cost of a semiconductor device as a whole.
[0040] Other manufacture approaches of the semiconductor device shown in above-mentioned drawing 1 are shown in drawing 3 . First, as shown in drawing 3 (a), on the silicon substrate 1 by which silicon oxide 7 is formed in the front face, the laminating of the polycrystalline silicon film 8, the silicon nitride 9, and the resist 10 is carried out to this order, patterning of the resist 10 is carried out using the usual photoengraving-process technique, and etching of the polycrystalline silicon film 8 and the silicon nitride 9 is performed by using as a mask this resist 10 by which patterning was carried out.
[0041] Next, as shown in drawing 3 (b), the LOCOS demarcation membrane 5 is formed in opening of the mask 36 of the silicon substrate 1 above-mentioned front face by oxidizing thermally the above-mentioned silicon substrate 1 using the mask 36 which consists of the polycrystalline silicon film 8 and the silicon nitride 9 by which etching was carried out [above-mentioned].
[0042] Next, as shown in drawing 3 (c), nitrogen ion 30b is poured in using the above-mentioned mask 36, and nitrogen impregnation layer 12b is formed in the bottom of the underside concerned near the underside of the above-mentioned LOCOS demarcation membrane 5. Here, the thickness of a mask 36 is the thickness which nitrogen ion 30b does not pass. .
[0043] Then, etching removes the above-mentioned mask 36 and the semiconductor device which has the silicon nitride layer 11 under the underside concerned near the underside of the above-mentioned LOCOS demarcation membrane 5 and which is shown in drawing 1 is obtained.
[0044] According to the manufacture approach of the semiconductor device shown in above-mentioned drawing 3 , the number of production processes of the semiconductor device which does not need to establish anew the photoengraving-process process for the mask formation for nitrogen ion 30b impregnation, therefore is shown in drawing 1 can be reduced.
[0045] And it has the effectiveness of enabling control of the thickness of the silicon nitride layer 11, the depth, nitrogen concentration, etc. for the redistribution of the impregnation nitrogen atom in the hot heat treatment process for formation of the LOCOS demarcation membrane 5 concerned not to happen, therefore to carry out easily after formation of the LOCOS demarcation membrane 5 compared with the case where nitrogen ion is poured in before formation of the LOCOS demarcation membrane 5 since the above-mentioned nitrogen ion 30b

is poured in.
[0046] When the impurity which forms the channel cut field which exists in the perimeter of the underside of the LOCOS demarcation membrane 5 is spread inside the LOCOS demarcation membrane 5 concerned and is conventionally absorbed inside by heat treatment etc., the high impurity concentration falls, therefore degradation of separation pressure-proofing, such as a punch-through phenomenon, is raw ******. Since it had especially the property in which the boron which is the impurity which forms a channel cut field is spread inside the LOCOS demarcation membrane 5 by heat treatment, and is easy to be absorbed, in the component isolation region of an N-channel metal oxide semiconductor transistor, the above-mentioned inclination was remarkable.
[0047] However, according to the semiconductor device shown in the gestalt 1 of operation of this invention, since the silicon nitride film 11 was formed in the bottom of the underside concerned near the underside of the LOCOS demarcation membrane 5, it becomes possible to be able to control and prevent diffusion inside the LOCOS demarcation membrane 5 of impurities, such as the above-mentioned boron, and absorption, therefore to prevent degradation of separation pressure-proofing.
[0048] Moreover, according to the semiconductor device shown in the gestalt 1 of operation of this invention, diffusion inside the LOCOS demarcation membrane 5 of the impurity concerned and absorption can be foreseen for impurities, such as boron for channel cut field formation, and it is not necessary to make [many] an injection rate beforehand, therefore the amount of impurities as the whole well field can be fallen, and reduction of a junction capacitance is attained.
[0049] Moreover, since the effectual thickness of a component isolation region becomes what added the thickness of the LOCOS demarcation membrane 5, and the thickness of the silicon nitride layer 11, it also becomes possible to reduce the wiring capacity of wiring of the word line formed in the upper layer of this LOCOS demarcation membrane 5.
[0050] Gestalt 2. drawing 4 of operation is the important section sectional view showing the gestalt 2 of implementation of this invention, and it is the same as that of the gestalt 1 of operation which is only different from the interior of the LOCOS demarcation membrane 5 concerned near the underside of the LOCOS demarcation membrane 5 at a point equipped with the nitriding silicon oxide layer 13, and was described above about other points instead of equipping the bottom of the underside concerned near the underside of the LOCOS demarcation membrane 5 with the silicon nitride layer 11 to the gestalt 1 of operation.
[0051] However, it sets in the gestalt 1 of operation as the manufacture approach of 1 of the semiconductor device concerned. As shown in drawing 2 (b), for impregnation of nitrogen ion 30a It sets in the gestalt 2 of this operation to using energy with which nitrogen impregnation layer 12a is formed in the bottom of the underside concerned near the underside of the LOCOS demarcation membrane 5. Energy with which nitrogen impregnation layer 12a is formed in the LOCOS demarcation membrane 5 interior concerned near the underside of the above-mentioned LOCOS demarcation membrane 5 is used for the impregnation energy of nitrogen ion 30a.
[0052] According to the manufacture approach of 1 of the semiconductor device concerned shown in above-mentioned drawing 2 , in the gestalt 2 of this operation, it is not necessary to establish anew the photoengraving-process process for the mask formation for nitrogen ion 30a impregnation. The sake, Since the above-mentioned nitrogen ion 30a is poured in before being able to reduce the number of production processes of the semiconductor device concerned and performing thermal oxidation for formation of the LOCOS demarcation membrane 5 moreover Compared with the case where nitrogen ion is poured in, the nitrogen ion implantation equipment of high energy is not needed after formation of the LOCOS demarcation membrane 5, but it becomes possible to reduce the manufacturing cost of a semiconductor device as a whole.
[0053] Moreover, it sets in the gestalt 1 of operation as other manufacture approaches of the semiconductor device concerned. As shown in drawing 3 (c), nitrogen ion 30b is poured in using the above-mentioned mask 36. In the gestalt 2 of this operation, nitrogen impregnation layer 12b is formed in the interior of the LOCOS demarcation membrane 5 concerned near the underside of the above-mentioned LOCOS demarcation membrane 5 to forming nitrogen impregnation layer

12b in the bottom of the underside concerned near the underside of the above-mentioned LOCOS demarcation membrane 5.
[0054] It is not necessary to establish anew the photoengraving-process process for the mask formation for nitrogen ion 30b impregnation, therefore, according to other manufacture approaches of the semiconductor device concerned shown in above-mentioned drawing 3 , the number of production processes of the semiconductor device concerned can be reduced also in the gestalt 2 of this operation.
[0055] And it has the effectiveness enable control of the thickness of the nitriding silicon oxide layer 13, the depth, nitrogen concentration, etc. for the redistribution of the impregnation nitrogen atom in the hot heat treatment process for formation of the LOCOS demarcation membrane 5 concerned not to happen, therefore to carry out easily after formation of the LOCOS demarcation membrane 5 compared with the case where nitrogen ion is poured in before formation of the LOCOS demarcation membrane 5 since the above-mentioned nitrogen ion 30b is poured in.
[0056] According to the semiconductor device shown in the gestalt 2 of operation of this invention, since the nitriding silicon oxide film 13 was formed in the interior of the LOCOS demarcation membrane 5 concerned near the underside of the LOCOS demarcation membrane 5, it becomes possible to be able to control and prevent diffusion inside the LOCOS demarcation membrane 5 of impurities, such as the above-mentioned boron, and absorption, therefore to prevent degradation of separation pressure-proofing.
[0057] Moreover, according to the semiconductor device shown in the gestalt 2 of operation of this invention, diffusion inside the LOCOS demarcation membrane 5 of the impurity concerned and absorption can be foreseen for impurities, such as boron for channel cut field formation, and it is not necessary to make [many] an injection rate beforehand, therefore the amount of impurities as the whole well field can be fallen, and reduction of a junction capacitance is attained.
[0058] Moreover, since according to the semiconductor device shown in the gestalt 2 of operation of this invention the nitriding silicon oxide layer 13 is formed near the underside of the LOCOS demarcation membrane 5 and the oxygen atom is contained in this nitriding silicon oxide layer 13, the difference of the expansion coefficient of a silicon substrate 1 and this nitriding silicon oxide layer 13 becomes it is small, therefore possible [suppressing small the leakage current by the stress produced in the interface of a silicon substrate 1 and the LOCOS demarcation membrane 5].
[0059] Gestalt 3. drawing 5 of operation is the important section sectional view showing the gestalt 3 of implementation of this invention, and receives the gestalt 1 of operation. Do not stop at forming the silicon nitride layer 11 only in the bottom of the underside concerned near the underside of the LOCOS demarcation membrane 5, but the silicon nitride layer 11 so that the underside of the LOCOS demarcation membrane 5 may be enclosed That is, it is the same as that of the gestalt 1 of operation which is only different at the point formed also in directly under [of a BAZU beak field], and was described above about other points.
[0060] However, instead of the process shown in above-mentioned drawing 2 (b) as the manufacture approach of 1 of the semiconductor device concerned using the manufacture approach shown by above-mentioned drawing 2 , as shown in drawing 6 , the process which performs impregnation of nitrogen ion 30c using a slanting revolution ion-implantation machine is used.
[0061] In order to form the mask for impregnation of nitrogen ion 30c by which a slanting revolution ion implantation is carried out also in the gestalt 3 of this operation according to the manufacture approach of the semiconductor device concerned shown in above-mentioned drawing 2 Since the above-mentioned nitrogen ion 30c is poured in before being able to reduce the number of production processes of the semiconductor device which does not need to establish a photoengraving-process process anew, therefore is shown in drawing 5 and performing thermal oxidation for formation of the LOCOS demarcation membrane 5 moreover Compared with the case where nitrogen ion is poured in, the nitrogen ion implantation equipment of high energy is not needed after formation of the LOCOS demarcation membrane 5, but it

becomes possible to reduce the manufacturing cost of a semiconductor device as a whole.
[0062] Since according to the semiconductor device shown in the gestalt 3 of operation of this invention the silicon nitride film 11 was formed so that the underside of the LOCOS demarcation membrane 5 might be surrounded, it becomes possible to be able to control and prevent diffusion inside the LOCOS demarcation membrane 5 of impurities, such as boron, and absorption, therefore to prevent degradation of separation pressure-proofing. It is effective in the ability to control and prevent diffusion inside the LOCOS demarcation membrane 5 of the impurity in directly under [BAZU beak], and absorption especially.
[0063] Moreover, according to the semiconductor device shown in the gestalt 3 of operation of this invention, diffusion inside the LOCOS demarcation membrane 5 of the impurity concerned and absorption can be foreseen for impurities, such as boron for channel cut field formation, and it is not necessary to make [many] an injection rate beforehand, therefore the amount of impurities as the whole well field can be fallen, and reduction of a junction capacitance is attained.
[0064] Moreover, according to the semiconductor device shown in the gestalt 3 of operation of this invention, in the field inserted into a mask 35 and nitrogen impregnation layer 12c at the time of that manufacture, a BAZU beak becomes not easily formed in the thermal oxidation process at the time of formation of the LOCOS demarcation membrane 5 of the stress from the nitrogen content layer of these upper and lower sides, therefore the high integration of a component of it is attained.
[0065] Gestalt 4. drawing 7 of operation is the important section sectional view showing the conventional semiconductor device, in drawing 7 , 1 is a silicon substrate, and 5a and 5b are LOCOS demarcation membranes which are the component detached cores which have different separation width of face W1 and W2 formed in this silicon substrate 1 front face. 14 is the channel cut field of a response in LOCOS demarcation membrane 5a, and is formed of the ion implantation which adjusted energy so that it might be formed in the bottom of the LOCOS demarcation membrane 5a concerned. On the other hand, 15 is a channel cut field corresponding to LOCOS demarcation membrane 5b, and is formed of the ion implantation which adjusted energy so that it might be formed in the bottom of the LOCOS demarcation membrane 5b concerned.
[0066] In the above-mentioned conventional semiconductor device, the thickness differs corresponding to each width of face of the LOCOS demarcation membranes 5a and 5b. Specifically by LOCOS demarcation membrane 5a with wide width of face, the thickness becomes thick compared with LOCOS demarcation membrane 5b with narrow width of face. If it is performing channel cut impregnation two or more times using the optimal impregnation energy corresponding to each of the LOCOS demarcation membranes 5a and 5b from which thickness's differs rather than managing one channel cut impregnation in order to form a channel cut field corresponding to the difference of this thickness, it will escape that separation pressure-proofing deteriorates in each LOCOS demarcation membrane 5a and 5b.
[0067] However, the problem that accumulation of the impurity by channel cut impregnation of multiple times will take place, and high impurity concentration will become large, therefore a junction capacitance will become large in this case in the bottom of LOCOS demarcation membrane 5b with narrow width of face had arisen.
[0068] Then, suppose that the gestalt 4 of operation of this invention for solving the above-mentioned problem is shown below.
[0069] The gestalt 4 of implementation of this invention is explained based on drawing 8 thru/or drawing 11 . Drawing 8 is the important section sectional view of 1 showing the gestalt 4 of operation of this invention, in drawing 8 , 1 is a silicon substrate, and 5c and 5d are LOCOS demarcation membranes which are the component detached cores which have different separation width of face W1 and W2 formed in this silicon substrate 1 front face. 40 is near [in which the above-mentioned LOCOS demarcation membranes 5c and 5d are formed among silicon substrate 1 front faces] the part, and is the field (it is hereafter called datum level.) which moreover extended the part in which the LOCOS demarcation membranes 5c and 5d concerned are not formed even to the concerned LOCOS detached cores [5c and 5d] interior.

[0070] As for x1 and x2, the thickness of the part above the LOCOS demarcation membranes [5c and 5d] datum level 40, and y1 and y2 are the thickness of the part below the LOCOS demarcation membranes [5c and 5d] datum level 40, and the above x1 and x2 have an almost equal value in the gestalt 4 of this operation. 16a is LOCOS demarcation membrane 5c and the channel cut field of a 5d response, and it is formed of one ion implantation which adjusted energy so that it may be formed in the bottom of the LOCOS demarcation membranes 5c and 5d concerned.
[0071] It sets to the semiconductor device shown by drawing 8 , and is LOCOS demarcation membrane 5c. Since it has an almost equal value, the thickness x1 of the part above the 5d datum level 40 and x2 are both LOCOS(s) demarcation membrane 5c. It becomes possible to suppress dimension dispersion of wiring of the word line formed in the 5d upper layer.
[0072] Below, the manufacture approach of the semiconductor device constituted in this way is explained using drawing 9 . Drawing 9 is the important section sectional view showing manufacture ****** of the semiconductor device shown in drawing 8 in order of a process.
[0073] First, as shown in drawing 9 (a), the laminating of the polycrystalline silicon film 8, the silicon nitride 9, and the resist 10 is carried out to this order like the manufacture approach of the conventional semiconductor device on the silicon substrate 1 by which silicon oxide 7 is formed in the front face. Carry out patterning of the resist 10 using the usual photoengraving-process technique, and etching of the polycrystalline silicon film 8 and the silicon nitride 9 is performed by using as a mask this resist 10 by which patterning was carried out. By oxidizing thermally the above-mentioned silicon substrate 1 using the mask 37 which consists of the polycrystalline silicon film 8 and the silicon nitride 9 by which etching was carried out [above-mentioned] The LOCOS demarcation membranes 5a and 5b which have separation width of face W1 and W2 which is different in opening of the mask 37 of the silicon substrate 1 above-mentioned front face are formed.
[0074] Next, as shown in drawing 9 (b), the LOCOS demarcation membranes 5c and 5d are formed by the dry etching using the above-mentioned mask 37 by making equal the thickness x1 of the part above datum level 40, and the value of x2 for the above-mentioned LOCOS demarcation membranes 5a and 5b.
[0075] Here, the micro [set at the process shown in above-mentioned drawing 9 (b), and / difference / in each LOCOS demarcation membranes / 5c and 5d / width of face] loading effects at the time of etching will differ, therefore the etching rates to each LOCOS demarcation membrane 5c and 5d will differ, and it becomes possible to make almost equal the thickness x1 of the part above datum level 40, and the value of x2.
[0076] The aspect ratio of opening of a mask 37 is set to about 2.5 in LOCOS demarcation membrane 5b whose thickness of 1000A and the silicon nitride 9 the thickness of 0.2 micrometers and the polycrystalline silicon film 8 is 4000A for the value of W2, and, specifically, lowering of the etching rate by the micro loading effect can be disregarded in LOCOS demarcation membrane 5a with the large value of W1 to the ability of lowering of the etching rate by the micro loading effect not to be disregarded.
[0077] Therefore, to the etching rate of LOCOS demarcation membrane 5c, the etching rate of 5d of LOCOS demarcation membranes becomes small, and it becomes possible to make almost equal the thickness x1 of the part above datum level 40, and the value of x2.
[0078] Then, the semiconductor device shown in drawing 8 is obtained by forming channel cut field 16a by one ion implantation which adjusted energy so that etching may remove the above-mentioned mask 37 and it may be formed in the bottom of both the LOCOS(s) demarcation membranes 5c and 5d.
[0079] Drawing 10 is other important section sectional views showing the gestalt 4 of operation of this invention, in drawing 10 , 1 is a silicon substrate, and 5e and 5f are LOCOS demarcation membranes which are the component detached cores which have different separation width of face W1 and W2 formed in this silicon substrate 1 front face.
[0080] z1 and z2 are LOCOS demarcation membranes [5e and 5f] thickness, and the above z1 and z2 has an almost equal value in the gestalt 4 of this operation. 16b is LOCOS demarcation membrane 5e and the channel cut field of a 5f response, and it is formed of one ion implantation

which adjusted energy so that it may be formed in the bottom of the LOCOS demarcation membranes 5e and 5f concerned.
[0081] Below, the manufacture approach of the semiconductor device constituted in this way is explained using drawing 11 . drawing 11 — < -- A HREF -- = -- " -- /-- Tokujitu/tjitemdrw . -- ipdl?N -- 0000 -- = -- 239 -- & -- N -- 0500 -- = -- one -- E_N -- /--; -- > -- ?? -- eight -- ? -- > -- > -- nine -- /-- /-- /-- & -- N -- 0001 -- = -- 109 -- & -- N -- 0552 -- = -- nine -- & -- N -- 0553 -- = -- 000012 -- " -- TARGET -- = -- "tjitemdrw" -- > -- drawing 10 -- being shown -- having -- a semiconductor device -- manufacture -- an approach -- a process -- order -- being shown -- an important section -- a sectional view -- it is -- .
[0082] First, as shown in drawing 11 (a), the laminating of the polycrystalline silicon film 8, the silicon nitride 9, and the resist 10 is carried out to this order like above-mentioned drawing 9 R> 9 (a) on the silicon substrate 1 by which silicon oxide 7 is formed in the front face. Carry out patterning of the resist 10 using the usual photoengraving-process technique, and etching of the polycrystalline silicon film 8 and the silicon nitride 9 is performed by using as a mask this resist 10 by which patterning was carried out. By oxidizing thermally the above-mentioned silicon substrate 1 using the mask 37 which consists of the polycrystalline silicon film 8 and the silicon nitride 9 by which etching was carried out [above-mentioned] The LOCOS demarcation membranes 5a and 5b which have separation width of face W1 and W2 which is different in opening of the mask 37 of the silicon substrate 1 above-mentioned front face are formed.
[0083] Next, as shown in drawing 11 (b), the LOCOS demarcation membranes 5e and 5f are formed by the dry etching using the above-mentioned mask 37 by making equal the value of the thickness z1 and z2 of the above-mentioned LOCOS demarcation membranes 5a and 5b.
[0084] Here, the reason which can make equal the value of thickness z1 and z2 originates in the difference in the etching rate by the above-mentioned micro loading effect, and becomes possible [making almost equal the value of thickness z1 and z2] from the condition by which it was shown by above-mentioned drawing 9 (b) by adding etching further.
[0085] Then, the semiconductor device shown in drawing 10 is obtained by forming channel cut field 16b by one ion implantation which adjusted energy so that etching may remove the above-mentioned mask 37 and it may be formed in the bottom of both the LOCOS(s) demarcation membranes 5e and 5f.
[0086] According to the semiconductor device shown in the gestalt 4 of operation of this invention, since the difference of the LOCOS demarcation membranes 5c and 5d or thickness (5e and 5f) can be made small, it becomes possible to form the channel cut field which has effective separation pressure-proofing by channel cut impregnation using 1 time of the optimal impregnation energy.
[0087] Therefore, it becomes unnecessary to perform channel cut impregnation of multiple times, the problem that accumulation of an impurity takes place is lost also in 5d of LOCOS demarcation membranes with narrow width of face, and the channel cut field under 5f, and it becomes possible as a result to stop a junction capacitance small.
[0088] The gestalt 5 of the operation of this invention for corresponding to the trouble shown with the gestalt 4 of gestalt 5. implementation of operation is explained below.
[0089] The gestalt 5 of implementation of this invention is explained based on drawing 12 and drawing 13 . Drawing 12 is the important section sectional view showing the gestalt 5 of operation of this invention, in drawing 12 , 1 is a silicon substrate, and 5a and 5b are LOCOS demarcation membranes which are the component detached cores which have different separation width of face W1 and W2 formed in this silicon substrate 1 front face. 17a and 17b are the BPSG film formed on LOCOS demarcation membrane 5a and 5b, respectively, and 5g and 5h are component detached cores formed from LOCOS demarcation membrane 5a, 5b and BPSG film 17a on it, or 17b. 40 is datum level.
[0090] t1 and t2 are the thickness of the part above the component detached cores [5g and 5h] datum level 40, and the above t1 and t2 has an almost equal value in the gestalt 5 of this operation. 16c is 5g of component detached cores, and the channel cut field of a 5h response, and it is formed of one ion implantation which adjusted energy so that it may be formed in the bottom of the component detached cores 5g and 5h concerned.

[0091] Below, the manufacture approach of the semiconductor device constituted in this way is explained using drawing 13 . Drawing 13 is the important section sectional view showing the gestalt 5 of this operation in order of a process.
[0092] First, as shown in drawing 13 (a), the laminating of the polycrystalline silicon film 8, the silicon nitride 9, and the resist 10 is carried out to this order like the manufacture approach of the conventional semiconductor device on the silicon substrate 1 by which silicon oxide 7 is formed in the front face. Carry out patterning of the resist 10 using the usual photoengraving-process technique, and etching of the polycrystalline silicon film 8 and the silicon nitride 9 is performed by using as a mask this resist 10 by which patterning was carried out. By oxidizing thermally the above-mentioned silicon substrate 1 using the mask 37 which consists of the polycrystalline silicon film 8 and the silicon nitride 9 by which etching was carried out [above-mentioned] The LOCOS demarcation membranes 5a and 5b which have separation width of face W1 and W2 which is different in opening of the mask 37 of the silicon substrate 1 above-mentioned front face are formed.
[0093] Next, as shown in drawing 13 (b), the insulator layer 17 which consists of BPSG film is deposited on a silicon substrate 1 on the whole surface. What is necessary is here, for flattening to be just possible for the insulator layer to deposit by the CMP method etc. not only in the above-mentioned BPSG film but a next process.
[0094] Next, it removes until it carries out flattening of the BPSG film 17 by the CMP method and the one section of the upper bed of a mask 37 is exposed, as shown in drawing 13 (c). Here, the approach of combining the etchback of O2 dry reflow processing and the BPSG film 17 may be used instead of the CMP method as an approach for exposing the one section of flattening of the BPSG film 17, and the upper bed of a mask 37.
[0095] then, H3 PO4 Perform used processing and the silicon nitride 9 which constitutes a mask 37, and the BPSG film 17 which remained a little on it are removed. etc. -- Then, the semiconductor device shown in drawing 12 is obtained by etching removing the polycrystalline silicon film 8, and forming channel cut field 16c by one ion implantation which adjusted energy so that it may finally be formed in the bottom of both the components detached cores 5e and 5f.
[0096] According to the semiconductor device shown in the gestalt 5 of operation of this invention, since the difference of component detached cores [5g and 5h] thickness can be made small, it becomes possible to form the channel cut field which has effective separation pressure-proofing by channel cut impregnation using 1 time of the optimal impregnation energy.
[0097] Therefore, it becomes unnecessary to perform channel cut impregnation of multiple times, the problem that accumulation of an impurity takes place is lost also in the channel cut field under LOCOS demarcation membrane 5b with narrow width of face, and it becomes possible as a result to stop a junction capacitance small.
[0098] Moreover, since according to the semiconductor device shown in the gestalt 5 of operation of this invention the difference of component detached cores [5g and 5h] thickness can be made small unlike the gestalt 4 of operation when the thickness of a mask 37 is thin, and when the difference in the etching rate by micro loading effects when the separation width of face W1 and W2 is comparatively wide does not take place, there is the description of having the above-mentioned effectiveness.
[0099] Gestalt 6. drawing 14 of operation is the important section sectional view showing the conventional semiconductor device, and 1 is a LOCOS demarcation membrane which is the component detached core by which a silicon substrate and 2 were formed in the P type well field, and 5 was formed in silicon substrate 1 front face in drawing 14 . 18 is an N type diffusion field currently formed all over the component formation field surrounded by the LOCOS demarcation membrane 5, and 19 expresses the side face of the diffusion field 18 of the side which touches the above-mentioned LOCOS demarcation membrane 5.
[0100] In the above-mentioned conventional semiconductor device, the problem that a touch area with the P type well 2 will be large, therefore a junction capacitance will become large had arisen in the side face 19 of an N type diffusion field.
[0101] Then, suppose that the gestalt 6 of operation of this invention for solving the above-mentioned problem is shown below.

[0102] The gestalt 6 of implementation of this invention is explained based on drawing 15 and drawing 16 . Drawing 15 is the important section sectional view showing the gestalt 6 of operation of this invention, and the well field where 1 shows a silicon substrate and 2 shows P type, and 20 are LOCOS demarcation membranes which are the component detached cores formed in silicon substrate 1 front face in drawing 15 . 40 is near [in which the above-mentioned LOCOS demarcation membrane 20 is formed among silicon substrate 1 front faces] the part. And the datum level which is a field which extended the part in which the LOCOS demarcation membrane 20 concerned is not formed even inside the LOCOS detached core 20 concerned, 18 is a diffusion field which is formed all over the component formation field surrounded by the LOCOS demarcation membrane 20 and which shows N type, for example, and 19 expresses the side face of the diffusion field 18 of the side which touches the above-mentioned LOCOS demarcation membrane 20 concerned.
[0103] Both of T1 and T2 are the thickness of the part below the datum level 40 of the LOCOS demarcation membrane 20, especially T1 expresses the above-mentioned thickness near the center of the LOCOS demarcation membrane 20, T2 expresses the above-mentioned thickness near the BAZU beak of the LOCOS demarcation membrane 20, and the above T1 and T2 has an almost equal value in the gestalt 6 of this operation. Moreover, in the gestalt 6 of this operation, most side faces 19 of a diffusion field have the description of being in contact with the LOCOS demarcation membrane 20.
[0104] Below, the manufacture approach of the semiconductor device constituted in this way is explained using drawing 16 . Drawing 16 is the important section sectional view showing manufacture ****** of the semiconductor device shown in drawing 15 in order of a process.
[0105] First, as shown in drawing 16 (a), the laminating of the polycrystalline silicon film 8, the silicon nitride 9, and the resist is carried out to this order like the manufacture approach of the conventional semiconductor device on the silicon substrate 1 by which silicon oxide 7 is formed in the front face. Carry out patterning of the resist using the usual photoengraving-process technique, and etching of the polycrystalline silicon film 8 and the silicon nitride 9 is performed by using as a mask this resist by which patterning was carried out. The mask 38 which consists of the polycrystalline silicon film 8 and the silicon nitride 9 by which etching was carried out [above-mentioned] is formed. Using this mask 38, the slanting revolution ion implantation of the oxygen ion 31 is carried out to a silicon substrate 1, and it is the lower part (this part is a part in which a BAZU beak is formed in a next process.) of a mask 38. The spreading oxygen impregnation layer 34 is formed in the semi-conductor substrate 1 interior.
[0106] Specifically, about 30-60 degrees is used [impregnation energy] for the injection rate of the oxygen ion 31 by the impregnation include angle using 30 - 100keV extent or more [1x1015cm -] using two. Here, oxygen ion will be injected even into the lower part of a mask 38 by using a slanting revolution ion implantation.
[0107] Next, as shown in drawing 16 (b), the LOCOS demarcation membrane 20 is formed in the above-mentioned silicon substrate surface by oxidizing the semi-conductor substrate 1 thermally using a mask 38. Here, of a slanting revolution ion implantation, since oxygen ion was injected even into the lower part of a mask 38, the LOCOS demarcation membrane 20 concerned will be formed so that the thickness T2 of the part below the datum level 40 near the BAZU beak of the above-mentioned LOCOS demarcation membrane 20 may become almost equal to the above-mentioned thickness T1 near a center.
[0108] Then, the semiconductor device shown in drawing 15 is obtained by etching removing the above-mentioned mask 38, forming the P type well field 2 by the ion implantation which stopped the injection rate low, and forming the N type diffusion field 18 in the component formation field surrounded by the LOCOS demarcation membrane 20.
[0109] Here, since the thickness T2 of the part below the datum level 40 of the LOCOS demarcation membrane 20 near a BAZU beak is formed almost like the above-mentioned thickness T1 near a center, as for the side face 19 of the diffusion field of the side which touches the above-mentioned LOCOS demarcation membrane 20, the most will touch the LOCOS demarcation membrane 20.
[0110] Therefore, according to the semiconductor device shown in the gestalt 6 of operation of

this invention, it becomes possible to be able to reduce the touch area of the N type diffusion field 18 and the P type well field 2, therefore to reduce a junction capacitance.
[0111] In addition, in the gestalt 6 of this operation, although the conductivity type of the diffusion field 18 was used as N type for the conductivity type of the well field 2 at P type, it is good mutually also as what has one of other conductivity types, and has the same effectiveness as the above also in this case.
[0112] Gestalt 7. drawing 17 of operation is the important section sectional view showing the gestalt 7 of operation of this invention, and in drawing 17 , 1 is a silicon substrate, and it is the LOCOS demarcation membrane which is the component detached core by which 2 was formed in the very low P type well field of high impurity concentration, and 5 was formed in silicon substrate 1 front face. 18 is an N type diffusion field where the high impurity concentration currently formed all over the N-channel MOS transistor formation field 41 surrounded by the LOCOS demarcation membrane 5 is high, and 21 is a P type channel cut field which was formed only in the bottom near the center of the LOCOS demarcation membrane 5 and which has high high impurity concentration compared with the well field 2.
[0113] In the semiconductor device shown in drawing 17 , in order not to make a junction capacitance increase, high impurity concentration of the well field 2 around the N type diffusion field 18 is made very low, but in one side, in order to prevent degradation of the separation pressure-proofing by the punch through condenser of the LOCOS demarcation membrane 5, the P type channel cut field 21 which has high high impurity concentration compared with the well field 2 is formed only in the bottom near the center of this LOCOS demarcation membrane 5.
[0114] In order to obtain the semiconductor device shown in drawing 17 , the manufacture approach shown in drawing 18 R> 8 is proposed. In the manufacture approach of the semiconductor device shown by drawing 18 , after that, the P type well field 2 is formed after forming the LOCOS demarcation membrane 5 in the front face of a silicon substrate 1, the resist mask 22 which carries out opening is formed near the center of the LOCOS demarcation membrane 5, it is pouring in the boron ion 32 using this mask 22, and the P type channel cut field 21 which has high high impurity concentration compared with that of the well field 2 is formed only in the bottom near the center of the LOCOS demarcation membrane 5.
[0115] However, by the manufacture approach of the semiconductor device shown by this drawing 18 , the photoengraving-process process for forming the mask 22 for formation of the channel cut field 21 is needed, and the problem that a manufacturing cost rises occurs.
[0116] Then, in the gestalt 7 of this operation, in order to solve the above-mentioned problem, a semiconductor device is manufactured using the manufacture approach shown in drawing 19 . As shown in drawing 19 (a), the LOCOS demarcation membrane 5 is first formed in the front face of the semi-conductor substrate 1 using the manufacture approach of the semiconductor device shown with the gestalt 2 of operation. Here, this LOCOS demarcation membrane 5 has the nitriding silicon oxide layer 13 near the underside of the LOCOS demarcation membrane 5 interior, as the gestalt 2 of operation showed. Then, the P type well field 2 where high impurity concentration is very low is formed in a silicon substrate 1 by the ion implantation.
[0117] Next, as shown in drawing 19 (b), the slanting revolution ion implantation of the boron ion 32a is carried out. The field 23 where the high impurity concentration of boron becomes high only in the bottom near the center of the LOCOS demarcation membrane 5 compared with that perimeter since a value with lower corresponding [rather than / as opposed to / at this time / a silicon substrate 1 / range / of boron ion 32a / projection] to the nitriding silicon oxide layer 13 is shown and the nitriding silicon oxide layer 13 exists near the underside inside [LOCOS demarcation membrane 5] the above is formed. It is because channel cut impregnation ion 32a from right and left will add and it will let only a part for the center section see.
[0118] Next, as shown in drawing 19 (c), by performing annealing treatment, the boron which is an impurity is re-diffused from the high-concentration impurity range 23, and the P type channel cut field 21 which has high high impurity concentration compared with the well field 2 is formed.
[0119] Then, the N type diffusion field 18 is formed in the N-channel MOS transistor formation field 41 surrounded by the LOCOS demarcation membrane 5 by the ion implantation, and the semiconductor device shown in drawing 17 is obtained.

[0120] In the manufacture approach of the semiconductor device shown in the gestalt 7 of operation of this invention, the photoengraving-process process for forming the mask for formation of the channel cut field 21 becomes unnecessary, and it has the effectiveness that a manufacturing cost can be reduced.
[0121] The gestalt 8 of implementation of this invention is explained below to gestalt 8. of operation based on drawing 20 and drawing 21 . Drawing 20 is the important section sectional view showing the gestalt 8 of operation of this invention, and in drawing 20 , 1 is a silicon substrate, and it is the LOCOS demarcation membrane which is the component detached core by which 2a was formed in the very low N type well field of high impurity concentration, and 5 was formed in silicon substrate 1 front face. 18a is a P type diffusion field where the high impurity concentration currently formed all over the P-channel MOS transistor formation field 42 surrounded by the LOCOS demarcation membrane 5 is high, and 21a is an N type channel cut field which was formed only in the bottom near the center of the LOCOS demarcation membrane 5 and which has high high impurity concentration compared with well field 2a.
[0122] In the semiconductor device shown in drawing 20 , in order not to make a junction capacitance increase, high impurity concentration of well field 2a around P type diffusion field 18a is made very low, but in one side, in order to prevent degradation of the separation pressure-proofing by the punch through condenser of the LOCOS demarcation membrane 5, N type channel cut field 21a which has high high impurity concentration compared with well field 2a is formed only in the bottom near the center of this LOCOS demarcation membrane 5.
[0123] Below, the manufacture approach of the semiconductor device constituted in this way is explained using drawing 21 . Drawing 21 is the important section sectional view showing the gestalt 8 of this operation in order of a process.
[0124] As shown in drawing 21 (a), first, the LOCOS demarcation membrane 5 is formed in the front face of the semi-conductor substrate 1 using the manufacture approach of the conventional LOCOS demarcation membrane, and high impurity concentration forms very low N type well field 2a in a silicon substrate 1 by the ion implantation. Then, the slanting revolution ion implantation of the phosphorus ion 33 is carried out. The field 24 where the high impurity concentration of Lynn becomes high only in the bottom near the center of the LOCOS demarcation membrane 5 compared with that perimeter since a value with lower corresponding to the LOCOS demarcation membrane 5 which consists [rather than / as opposed to / at this time / a silicon substrate 1 / range / of the phosphorus ion 33 / projection] of a silicon oxide layer is shown is formed. Only the amount of the center section is because the channel cut impregnation ion 33 from right and left will add and it will let it see.
[0125] Next, as shown in drawing 21 (b), by performing annealing treatment, Lynn which is an impurity is re-diffused from the high-concentration impurity range 24, and N type channel cut field 21a which has high high impurity concentration compared with well field 2a is formed.
[0126] Then, P type diffusion field 18a is formed in the P-channel MOS transistor formation field 42 surrounded by the LOCOS demarcation membrane 5 by the ion implantation, and the semiconductor device shown in drawing 20 is obtained.
[0127] In the manufacture approach of the semiconductor device shown in the gestalt 8 of operation of this invention, the photoengraving-process process for forming the mask for formation of channel cut field 21a becomes unnecessary, and it has the effectiveness that a manufacturing cost can be reduced.
[0128] The manufacture approach of the semiconductor device shown by above-mentioned drawing 17 which is the gestalt 9 of implementation of this invention is explained below to gestalt 9. of operation based on drawing 22 . Drawing 22 is the important section sectional view showing the gestalt 9 of operation of this invention in order of a process.
[0129] First, as shown in drawing 22 (a), the LOCOS demarcation membrane 5 is formed in silicon substrate 1 front face by oxidizing a silicon substrate 1 thermally by the manufacture approach of the conventional LOCOS demarcation membrane using the mask 39 which consists of polycrystalline silicon film 8 and a silicon nitride 9.
[0130] Next, as shown in drawing 22 (b), a sidewall 25 is formed in the side attachment wall of a mask 39 by applying and carrying out etchback of the resist the whole surface on a silicon

substrate 1.
[0131] What is necessary is here, to use the usual photoengraving-process technique, to carry out patterning of the resist, and just to cover one upper part of the appointed field concerned by the resist, before performing etchback of the above-mentioned resist when a P type field and an N type field need to be specified, respectively by performing channel cut impregnation at degree process using a conductivity type different, respectively. However, where a limit of time amount assignment etc. is prepared, the above-mentioned etchback is performed so that it may not remove in this case to the resist which has covered the appointed field at the time of the etchback of the above-mentioned resist.
[0132] Next, as shown in drawing 22 (c), boron ion 32b is poured in by using the above-mentioned sidewall 25 as a mask, and the P type channel cut field 21 is formed only in the bottom near the center of the LOCOS demarcation membrane 5.
[0133] Next, as shown in drawing 22 (d), wet processing removes the above-mentioned sidewall 25.
[0134] Then, the well field 2 which has low high impurity concentration compared with the channel cut field 21 in a silicon substrate 1 is formed by the ion implantation, the N type diffusion field 18 is formed in the N-channel MOS transistor formation field 41 surrounded by the LOCOS demarcation membrane 5, and the semiconductor device shown in drawing 17 is obtained.
[0135] Since degradation of the separation pressure-proofing by the punch through condenser of the LOCOS demarcation membrane 5 can be prevented since the P type channel cut field 21 which has high high impurity concentration compared with the well field 2 is formed only in the bottom near the center of the LOCOS demarcation membrane 5, and high impurity concentration of the well field 2 around the N type diffusion field 18 is moreover made very low, a junction capacitance is not made to increase in the semiconductor device formed as mentioned above.
[0136] Moreover, it is not necessary to carry out alignment of the sidewall 25 which is a mask for formation of the channel cut field 21 anew, and it becomes possible to form a mask 25 in self align, so that the P type channel cut field 21 can be formed only in the bottom near the center of the LOCOS demarcation membrane 5 in the manufacture approach of the semiconductor device shown in the gestalt 9 of operation of this invention.
[0137] Moreover, in the manufacture approach of the semiconductor device shown in the gestalt 9 of operation of this invention, it has the effectiveness that it is not necessary to carry out a slanting revolution ion implantation, therefore a manufacturing cost can be reduced for formation of the channel cut field 21.
[0138] And since the above-mentioned boron ion 32b is poured in after formation of the LOCOS demarcation membrane 5, compared with the case where boron ion is poured in before formation of the LOCOS demarcation membrane 5, the redistribution of the impregnation boron atom in the hot heat treatment process for formation of the LOCOS demarcation membrane 5 concerned has an advantage of ********.
[0139] In addition, in the gestalt 9 of this operation, although the conductivity type of the diffusion field 18 was used as N type for the conductivity type of the well field 2 and the channel cut field 21 at P type, it is good mutually also as what has one of other conductivity types, and has the same effectiveness as the above also in this case.
[0140] The manufacture approach of the semiconductor device shown by above-mentioned drawing 17 which is the gestalt 10 of implementation of this invention is explained below to gestalt 10. of operation based on drawing 23 . Drawing 23 is the important section sectional view showing the gestalt 10 of operation of this invention in order of a process.
[0141] First, as shown in drawing 23 (a), on the silicon substrate 1 by which silicon oxide 7 is formed in the front face, the laminating of the polycrystalline silicon film 8, the silicon nitride 9, and the resist is carried out to this order, patterning of the resist is carried out using the usual photoengraving-process technique, etching of the polycrystalline silicon film 8 and the silicon nitride 9 is performed by using as a mask this resist by which patterning was carried out, and the mask 39 which consists of the polycrystalline silicon film 8 and the silicon nitride 9 by which etching was carried out [above-mentioned] is formed.

[0142] Next, as shown in drawing 23 (b), a sidewall 26 is formed in the side attachment wall of a mask 39 by applying and carrying out etchback of the resist the whole surface on a silicon substrate 1.
[0143] What is necessary is here, to use the usual photoengraving-process technique, to carry out patterning of the resist, and just to cover one upper part of the appointed field concerned by the resist, before performing etchback of the above-mentioned resist when a P type field and an N type field need to be specified, respectively by performing channel cut impregnation at degree process using a conductivity type different, respectively. However, where a limit of time amount assignment etc. is prepared, the above-mentioned etchback is performed so that it may not remove in this case to the resist which has covered the appointed field at the time of the etchback of the above-mentioned resist.
[0144] Moreover, as construction material of the above-mentioned sidewall 26, it may replace with the above-mentioned resist, and construction material with the selection ratio higher than the polycrystalline silicon film 8 and the silicon nitride 9 to dry etching may be used, and the construction material in which clearance by wet processing is possible may be used here.
[0145] Next, as shown in drawing 23 (c), boron ion 32c is poured in by using the above-mentioned sidewall 26 as a mask, and the P type channel cut field 21 is formed so that it may be located only under near the center of the LOCOS demarcation membrane 5 formed in subsequent processes.
[0146] Next, as shown in drawing 23 (d), wet processing removes the above-mentioned sidewall 26.
[0147] Next, as shown in drawing 23 (e), the LOCOS demarcation membrane 5 is formed in right above [of silicon substrate 1 front face / above-mentioned / P type channel cut field 21] by oxidizing thermally using the mask 39 which consists of polycrystalline silicon film 8 and a silicon nitride 9.
[0148] Then, the well field 2 which has low high impurity concentration compared with the channel cut field 21 in a silicon substrate 1 is formed by the ion implantation, the N type diffusion field 18 is formed in the N-channel MOS transistor formation field 41 surrounded by the LOCOS demarcation membrane 5, and the semiconductor device shown in drawing 17 is obtained.
[0149] Since degradation of the separation pressure-proofing by the punch through condenser of the LOCOS demarcation membrane 5 can be prevented since the P type channel cut field 21 which has high high impurity concentration compared with the well field 2 is formed only in the bottom near the center of the LOCOS demarcation membrane 5, and high impurity concentration of the well field 2 around the N type diffusion field 18 is moreover made very low, a junction capacitance is not made to increase in the semiconductor device formed as mentioned above.
[0150] Moreover, it is not necessary to carry out alignment of the sidewall 26 which is a mask for formation of the channel cut field 21 anew, and it becomes possible to form a mask 26 in self align, so that the P type channel cut field 21 can be formed only in the bottom near the center of the LOCOS demarcation membrane 5 in the manufacture approach of the semiconductor device shown in the gestalt 10 of operation of this invention.
[0151] Moreover, in the manufacture approach of the semiconductor device shown in the gestalt 10 of operation of this invention, it has the effectiveness that it is not necessary to carry out a slanting revolution ion implantation, therefore a manufacturing cost can be reduced for formation of the channel cut field 21.
[0152] And since the above-mentioned boron ion 32c is poured in before performing thermal oxidation for formation of the LOCOS demarcation membrane 5, compared with the case where boron ion is poured in, the boron ion implantation equipment of high energy is not needed after formation of the LOCOS demarcation membrane 5, but it becomes possible to reduce the manufacturing cost of a semiconductor device as a whole.
[0153] In addition, in the gestalt 10 of this operation, although the conductivity type of the diffusion field 18 was used as N type for the conductivity type of the well field 2 and the channel cut field 21 at P type, it is good mutually also as what has one of other conductivity types, and has the same effectiveness as the above also in this case.

[0154]
[Effect of the Invention] The semiconductor device concerning this invention by oxidation of the silicon substrate concerned using the mask formed on the front face of a silicon substrate Since the component detached core formed in the above-mentioned silicon substrate surface and the nitrogen content layer formed near the underside of the above-mentioned component detached core of the ion implantation of the nitrogen to the above-mentioned silicon substrate using the above-mentioned mask were prepared It is not necessary to carry out the ion implantation of the amount of ion implantations of a channel cut to the part which applied the amount of extrusion of the impurity ion to the above-mentioned component detached core beforehand. The sake, The impurities in a well can be reduced as a whole, and, therefore, it has the effectiveness that the junction capacitance in the semiconductor device concerned can be reduced.
[0155] It has the component detached core formed in the semi-conductor substrate front face. Moreover, the inside of the above-mentioned semi-conductor substrate front face, Are near [in which the component detached core concerned is formed] the part, and the field which extended the part in which the above-mentioned component detached core is not formed even inside the component detached core concerned is made into datum level. While the above-mentioned component detached core has two or more fields where the width of face in the vertical section to the above-mentioned datum level differs It has the effectiveness that optimization of impregnation energy of the ion implantation for forming a channel cut field regardless of the width of face since thickness is almost fixed is easy, therefore the junction capacitance in the semiconductor device concerned can be reduced.
[0156] It has the component detached core formed in the semi-conductor substrate front face. Moreover, the inside of the above-mentioned semi-conductor substrate front face, Are near [in which the component detached core concerned is formed] the part, and the field which extended the part in which the above-mentioned component detached core is not formed even inside the component detached core concerned is made into datum level. While the above-mentioned component detached core has two or more fields where the width of face in the vertical section to the above-mentioned datum level differs Regardless of the width of face, since the thickness of the part above the above-mentioned datum level is almost fixed Optimization of impregnation energy of the ion implantation for forming a channel cut field is easy. The sake, It has the effectiveness that the junction capacitance in the semiconductor device concerned can be reduced, and also has the effectiveness that dispersion in the dimension of wiring formed on the above-mentioned component detached core can be lessened further.
[0157] Moreover, while being formed in the field surrounded by the above-mentioned component detached core of the field in which the component detached core formed in the front face of a semi-conductor substrate and the component detached core of the above-mentioned semi-conductor substrate are formed It has the diffusion field in which the side face is in contact with the above-mentioned component detached core. The inside of the above-mentioned semi-conductor substrate front face, It is near [in which the component detached core concerned is formed] the part, and the field which extended the part in which the above-mentioned component detached core is not formed even inside the component detached core concerned is made into datum level. The above-mentioned component detached core The thickness of the part below the above-mentioned datum level to kick is about 1 law. the vertical section to this datum level -- setting -- the vertical section concerned -- the above-mentioned diffusion field Since most side faces which are in contact with the above-mentioned component detached core are in contact with the component detached core concerned, it has the effectiveness that the touch area of the diffusion field and well concerned in the side face of the above-mentioned diffusion field can be reduced, therefore the junction capacitance in the semiconductor device concerned can be reduced.
[0158] The manufacture approach of the semiconductor device concerning this invention carries out the laminating of the polycrystalline silicon film, a silicon nitride, and the resist to this order on the silicon substrate by which silicon oxide was formed in the front face. The process which forms a mask, and the process which carries out the ion implantation of the nitrogen to the

above-mentioned silicon substrate using the above-mentioned mask, Since the process which removes the resist which are some above-mentioned masks, and the process which oxidizes the above-mentioned silicon substrate thermally using the mask from which the above-mentioned resist was removed are provided It is not necessary to establish anew the photoengraving-process process for carrying out the ion implantation of the nitrogen, therefore has the effectiveness that a routing counter is reducible, and since the ion-implantation machine of high energy is still more unnecessary, it also has the effectiveness that it is possible to hold down a manufacturing cost low.

[0159] Moreover, the laminating of the polycrystalline silicon film and the silicon nitride is carried out to this order on the silicon substrate by which silicon oxide was formed in the front face. Since the process which forms a mask, the process which oxidizes the above-mentioned silicon substrate thermally using the above-mentioned mask, and the process which carries out the ion implantation of the nitrogen to the above-mentioned silicon substrate using the above-mentioned mask are provided It is not necessary to establish anew the photoengraving-process process for carrying out the ion implantation of the nitrogen. The sake, It has the effectiveness that a routing counter is reducible, and further, diffusion of the nitrogen by the above-mentioned heat treatment does not arise, but it has the effectiveness that control of the content of the nitrogen in control of the thickness of a silicon nitride layer or a nitriding silicon oxide layer and the above-mentioned silicon nitride layer, or a nitriding silicon oxide layer and the depth is easy.

[0160] [oxidize / the above-mentioned semi-conductor substrate / the process which forms a mask on the front face of a semi-conductor substrate, and / moreover, / thermally / using the above-mentioned mask] Since the process which forms a component detached core, and the process which carries out dry etching of the above-mentioned component detached core using the above-mentioned mask are provided Also when the aperture width of the mask which forms the above-mentioned component detached core differs, since the rates of the dry etching to each component detached core differ, according to a difference of the micro loading effect by the difference in the aperture width of the mask it has the effectiveness that the component detached core concerned can be formed in the thickness of about 1 law regardless of the aperture width of the above-mentioned mask.

[0161] [oxidize / the above-mentioned semi-conductor substrate / the process which forms a mask on the front face of a semi-conductor substrate, and / moreover, / thermally / using the above-mentioned mask] Until a part of the process which forms a component detached core, process which forms an insulator layer on the above-mentioned semi-conductor substrate, process which carries out flattening of the above-mentioned insulator layer, and upper bed of the above-mentioned mask are exposed Since the process which removes the insulator layer which carried out [above-mentioned] flattening, and the process which removes the above-mentioned mask are provided Also when the aperture width of the mask which forms the above-mentioned component detached core differs, regardless of the aperture width of the above-mentioned mask Are near [in which the component detached core concerned is formed among the above-mentioned semi-conductor substrate front faces] the part, and the field which extended the part in which the above-mentioned component detached core is not formed even inside the component detached core concerned is made into datum level: it has the effectiveness that the part above the above-mentioned datum level of the component detached core concerned can be formed in the thickness of about 1 law.

[0162] Moreover, the laminating of the polycrystalline silicon film and the silicon nitride is carried out to this order on the silicon substrate by which silicon oxide was formed in the front face. Since the process which forms a mask, the process which carries out the slanting revolution ion implantation of the oxygen to the above-mentioned silicon substrate using the above-mentioned mask, and the process which oxidizes the above-mentioned silicon substrate thermally using the above-mentioned mask are provided Are near the component detached core formed of the above-mentioned thermal oxidation among the above-mentioned semi-conductor substrate front faces, and the field which extended the part which does not have this component detached core formation even inside the component detached core concerned is made into datum level. in the vertical section of the component detached core concerned to the above-mentioned datum

level, it has the effectiveness that the part below the above-mentioned datum level in the vertical section concerned can be formed in the thickness of about 1 law.
[0163] Moreover, since the process which forms a component detached core in one principal plane of a silicon substrate, and the process which forms a channel cut field by carrying out the slanting revolution ion implantation of Lynn to one principal plane of the above-mentioned silicon substrate are provided It is directly under the above-mentioned component isolation region, and concentration of Lynn near the center of the component isolation region concerned can be made high. The sake, It has the effectiveness that a semiconductor device with a low junction capacitance can be formed, and it is not necessary to form a mask anew for the ion implantation of above-mentioned Lynn, and has further the effectiveness that simplification of a production process can be attained.
[0164] Moreover, since the process which forms in one principal plane of a silicon substrate the component detached core which has a nitriding silicon oxide layer, and the process which forms a channel cut field by carrying out the slanting revolution ion implantation of the boron to one principal plane of the above-mentioned silicon substrate are provided It is directly under the above-mentioned component isolation region, and concentration of the boron near the center of the component isolation region concerned can be made high. The sake, It has the effectiveness that a semiconductor device with a low junction capacitance can be formed, and it is not necessary to form a mask anew for the ion implantation of the above-mentioned boron, and has further the effectiveness that simplification of a production process can be attained.
[0165] Moreover, the laminating of the polycrystalline silicon film and the silicon nitride is carried out to this order on the silicon substrate by which silicon oxide was formed in the front face. The process which forms a mask, and the process which oxidizes the above-mentioned silicon substrate thermally using the above-mentioned mask, The process which forms in the above-mentioned mask side face the sidewall which consists of a resist, Since the process which carries out the ion implantation of the impurity to the interior of the above-mentioned silicon substrate by using the above-mentioned sidewall as a mask, and the process which removes the above-mentioned sidewall by etching are provided High impurity concentration of the channel cut field located near the center of the component isolation region [directly under] of the above-mentioned component isolation region concerned can be made high, therefore it has the effectiveness that a semiconductor device with a low junction capacitance can be formed.
[0166] Moreover, the laminating of the polycrystalline silicon film and the silicon nitride is carried out to this order on the silicon substrate by which silicon oxide was formed in the front face. The process which forms a mask, and the process which forms in the side face of the above-mentioned mask the sidewall which consists of a resist, The process which carries out the ion implantation of the impurity to the interior of the above-mentioned silicon substrate by using the above-mentioned sidewall as a mask, Since the process which removes the above-mentioned sidewall by etching, and the process which oxidizes the above-mentioned silicon substrate thermally using the mask which consists of the above-mentioned polycrystalline silicon film and a silicon nitride are provided High impurity concentration of the channel cut field located near the center of the component isolation region [directly under] of the above-mentioned component isolation region concerned can be made high, therefore it has the effectiveness that a semiconductor device with a low junction capacitance can be formed.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Field of the Invention] It is related with LOCOS (LocalOxidation of Silicon) which is a technique for this invention to perform electric separation between two or more component formation fields especially about the structure and its manufacture approach of a semiconductor device.

[Translation done.]

PRIOR ART

[Description of the Prior Art] Conventionally, LOCOS (Local Oxidation of Silicon) has been widely used as the formation approach of the separation oxide film used for the isolation of a semiconductor integrated circuit. However, when Above LOCOS was used with detailed-izing of a semiconductor device, it had become the factor which occupies the area of a component formation field in an excess, consequently resists integration of a semiconductor circuit because lateral oxidization progresses beyond the need and a BAZU beak occurs. Then, Poly-Si using the mask of the structure which sandwiched the polycrystalline silicon film between silicon oxide and a silicon nitride in order to control this BAZU beak length in recent years buffered LOCOS (hereafter referred to as PBL.) is used increasingly.
[0003] The structure of the semiconductor device equipped with the separation oxide film which used PBL below and was formed in the silicon substrate surface, and the impurity range formed in the silicon substrate using the conventional manufacture approach is explained using drawing 24 and drawing 25 .
[0004] Drawing 24 is the important section sectional view showing the structure of the conventional semiconductor device, and is set to drawing 24 . The well field where 1 was formed in the silicon substrate and 2 was formed in one principal plane of a silicon substrate 1, The channel cut field formed in the part with 3 [shallower than the above-mentioned well field 2 of the principal plane of a silicon substrate 1], The channel dope field where 4 was formed in the component formation field 6 near the front face of a silicon substrate 1, 5 is formed so that the perimeter of the component formation field 6 may be surrounded, it separates electrically each of two or more component formation fields 6, for example, is a separation oxide film (LOCOS demarcation membrane) which has about 4000A thickness.
[0005] Drawing 25 is the important section sectional view showing the manufacture approach of the conventional semiconductor device in order of a process. first, the thing oxidized in silicon substrate 1 front face as shown in drawing 25 (a) -- for example, the silicon oxide 7 of about 50-500A thickness -- forming -- this silicon oxide 7 top -- for example, polycrystalline silicon film 8a of about 100-1000A thickness and about 500-4000A thickness -- having -- a presentation -- Si3 N4 it is -- silicon nitride 9a is deposited on this order. Here, silicon oxide 7 may be formed with a CVD method.
[0006] Next, as shown in drawing 25 (b), while applying a resist on a silicon substrate 1 and carrying out patterning of the resist concerned using the usual photoengraving-process technique, using the resist 10 by which patterning was carried out, sequential etching of above-mentioned silicon nitride 9a and the polycrystalline silicon film 8a is carried out, and the mask which consists of the silicon nitride 9 and the polycrystalline silicon film 8 is formed. .
[0007] Next, as shown in drawing 25 (c), a resist 10 is removed, a silicon substrate 1 is oxidized thermally using the mask which consists of polycrystalline silicon film 8 and a silicon nitride 9, and the separation oxide film 5 which is a LOCOS demarcation membrane is formed. Then, etching removes the polycrystalline silicon film 8 and the silicon nitride 9.
[0008] Next, as shown in drawing 25 (d), the ion implantation (well impregnation) of the impurity 27 for forming the well field 2 is performed, and impurity range 2a used as the well field 2 is formed in a silicon substrate 1. Here, although energy which is with the case of P type well

formation and the case of N type well formation, and is different among the generations of a manufacture process, respectively is used for impregnation energy, specifically, the high energy of 100 - 2000keV extent is used for it.

[0009] Next, as shown in drawing 25 (e), the ion implantation (channel cut impregnation) of the impurity 28 for forming the channel cut field 3 is performed, and impurity range 3a used as the channel cut field 3 is formed. Here, specifically, the energy of 100 - 1000keV extent is used for impregnation energy. In order to separate electrically each of two or more component formation fields 6, this channel cut impregnation pours in the impurity of the same conductivity type as well impregnation so that impurity range 3a may be formed directly under the separation oxide film 5.

[0010] Next, as shown in drawing 25 (f), the ion implantation (channel dope impregnation) of the impurity 29 for forming the channel dope field 4 is performed, and impurity range 4a used as the channel dope field 4 is formed. Here, specifically, the energy of 5 - 100keV extent is used for impregnation energy. This channel dope impregnation is poured in near the front face of a silicon substrate 1, in order to control threshold electrical potential differences, such as an MOS transistor formed in the component formation field 6.

[0011] Then, the semiconductor device shown by drawing 24 is obtained through processes, such as annealing treatment.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] The semiconductor device concerning this invention by oxidation of the silicon substrate concerned using the mask formed on the front face of a silicon substrate Since the component detached core formed in the above-mentioned silicon substrate surface and the nitrogen content layer formed near the underside of the above-mentioned component detached core of the ion implantation of the nitrogen to the above-mentioned silicon substrate using the above-mentioned mask were prepared It is not necessary to carry out the ion implantation of the amount of ion implantations of a channel cut to the part which applied the amount of extrusion of the impurity ion to the above-mentioned component detached core beforehand. The sake, The impurities in a well can be reduced as a whole, and, therefore, it has the effectiveness that the junction capacitance in the semiconductor device concerned can be reduced.
[0155] It has the component detached core formed in the semi-conductor substrate front face. Moreover, the inside of the above-mentioned semi-conductor substrate front face, Are near [in which the component detached core concerned is formed] the part, and the field which extended the part in which the above-mentioned component detached core is not formed even inside the component detached core concerned is made into datum level. While the above-mentioned component detached core has two or more fields where the width of face in the vertical section to the above-mentioned datum level differs It has the effectiveness that optimization of impregnation energy of the ion implantation for forming a channel cut field regardless of the width of face since thickness is almost fixed is easy, therefore the junction capacitance in the semiconductor device concerned can be reduced.
[0156] It has the component detached core formed in the semi-conductor substrate front face. Moreover, the inside of the above-mentioned semi-conductor substrate front face, Are near [in which the component detached core concerned is formed] the part, and the field which extended the part in which the above-mentioned component detached core is not formed even inside the component detached core concerned is made into datum level. While the above-mentioned component detached core has two or more fields where the width of face in the vertical section to the above-mentioned datum level differs Regardless of the width of face, since the thickness of the part above the above-mentioned datum level is almost fixed Optimization of impregnation energy of the ion implantation for forming a channel cut field is easy. The sake, It has the effectiveness that the junction capacitance in the semiconductor device concerned can be reduced, and also has the effectiveness that dispersion in the dimension of wiring formed on the above-mentioned component detached core can be lessened further.
[0157] Moreover, while being formed in the field surrounded by the above-mentioned component detached core of the field in which the component detached core formed in the front face of a semi-conductor substrate and the component detached core of the above-mentioned semi-conductor substrate are formed It has the diffusion field in which the side face is in contact with the above-mentioned component detached core. The inside of the above-mentioned semi-conductor substrate front face, It is near [in which the component detached core concerned is formed] the part, and the field which extended the part in which the above-mentioned component detached core is not formed even inside the component detached core concerned is

made into datum level. The above-mentioned component detached core The thickness of the part below the above-mentioned datum level to kick is about 1 law. the vertical section to this datum level -- setting -- the vertical section concerned -- the above-mentioned diffusion field Since most side faces which are in contact with the above-mentioned component detached core are in contact with the component detached core concerned, it has the effectiveness that the touch area of the diffusion field and well concerned in the side face of the above-mentioned diffusion field can be reduced, therefore the junction capacitance in the semiconductor device concerned can be reduced.

[0158] The manufacture approach of the semiconductor device concerning this invention carries out the laminating of the polycrystalline silicon film, a silicon nitride, and the resist to this order on the silicon substrate by which silicon oxide was formed in the front face. The process which forms a mask, and the process which carries out the ion implantation of the nitrogen to the above-mentioned silicon substrate using the above-mentioned mask, Since the process which removes the resist which are some above-mentioned masks, and the process which oxidizes the above-mentioned silicon substrate thermally using the mask from which the above-mentioned resist was removed are provided It is not necessary to establish anew the photoengraving-process process for carrying out the ion implantation of the nitrogen, therefore has the effectiveness that a routing counter is reducible, and since the ion-implantation machine of high energy is still more unnecessary, it also has the effectiveness that it is possible to hold down a manufacturing cost low.

[0159] Moreover, the laminating of the polycrystalline silicon film and the silicon nitride is carried out to this order on the silicon substrate by which silicon oxide was formed in the front face. Since the process which forms a mask, the process which oxidizes the above-mentioned silicon substrate thermally using the above-mentioned mask, and the process which carries out the ion implantation of the nitrogen to the above-mentioned silicon substrate using the above-mentioned mask are provided It is not necessary to establish anew the photoengraving-process process for carrying out the ion implantation of the nitrogen. The sake, It has the effectiveness that a routing counter is reducible, and further, diffusion of the nitrogen by the above-mentioned heat treatment does not arise, but it has the effectiveness that control of the content of the nitrogen in control of the thickness of a silicon nitride layer or a nitriding silicon oxide layer and the above-mentioned silicon nitride layer, or a nitriding silicon oxide layer and the depth is easy.

[0160] [oxidize / the above-mentioned semi-conductor substrate / the process which forms a mask on the front face of a semi-conductor substrate, and / moreover, / thermally / using the above-mentioned mask] Since the process which forms a component detached core, and the process which carries out dry etching of the above-mentioned component detached core using the above-mentioned mask are provided Also when the aperture width of the mask which forms the above-mentioned component detached core differs, since the rates of the dry etching to each component detached core differ, according to a difference of the micro loading effect by the difference in the aperture width of the mask it has the effectiveness that the component detached core concerned can be formed in the thickness of about 1 law regardless of the aperture width of the above-mentioned mask.

[0161] [oxidize / the above-mentioned semi-conductor substrate / the process which forms a mask on the front face of a semi-conductor substrate, and / moreover, / thermally / using the above-mentioned mask] Until a part of the process which forms a component detached core, process which forms an insulator layer on the above-mentioned semi-conductor substrate, process which carries out flattening of the above-mentioned insulator layer, and upper bed of the above-mentioned mask are exposed Since the process which removes the insulator layer which carried out [above-mentioned] flattening, and the process which removes the above-mentioned mask are provided Also when the aperture width of the mask which forms the above-mentioned component detached core differs, regardless of the aperture width of the above-mentioned mask Are near [in which the component detached core concerned is formed among the above-mentioned semi-conductor substrate front faces] the part, and the field which extended the part in which the above-mentioned component detached core is not formed even inside the component detached core concerned is made into datum level. it has the

effectiveness that the part above the above-mentioned datum level of the component detached core concerned can be formed in the thickness of about 1 law.
[0162] Moreover, the laminating of the polycrystalline silicon film and the silicon nitride is carried out to this order on the silicon substrate by which silicon oxide was formed in the front face. Since the process which forms a mask, the process which carries out the slanting revolution ion implantation of the oxygen to the above-mentioned silicon substrate using the above-mentioned mask, and the process which oxidizes the above-mentioned silicon substrate thermally using the above-mentioned mask are provided Are near the component detached core formed of the above-mentioned thermal oxidation among the above-mentioned semi-conductor substrate front faces, and the field which extended the part which does not have this component detached core formation even inside the component detached core concerned is made into datum level. in the vertical section of the component detached core concerned to the above-mentioned datum level, it has the effectiveness that the part below the above-mentioned datum level in the vertical section concerned can be formed in the thickness of about 1 law.
[0163] Moreover, since the process which forms a component detached core in one principal plane of a silicon substrate, and the process which forms a channel cut field by carrying out the slanting revolution ion implantation of Lynn to one principal plane of the above-mentioned silicon substrate are provided It is directly under the above-mentioned component isolation region, and concentration of Lynn near the center of the component isolation region concerned can be made high. The sake, It has the effectiveness that a semiconductor device with a low junction capacitance can be formed, and it is not necessary to form a mask anew for the ion implantation of above-mentioned Lynn, and has further the effectiveness that simplification of a production process can be attained.
[0164] Moreover, since the process which forms in one principal plane of a silicon substrate the component detached core which has a nitriding silicon oxide layer, and the process which forms a channel cut field by carrying out the slanting revolution ion implantation of the boron to one principal plane of the above-mentioned silicon substrate are provided It is directly under the above-mentioned component isolation region, and concentration of the boron near the center of the component isolation region concerned can be made high. The sake, It has the effectiveness that a semiconductor device with a low junction capacitance can be formed, and it is not necessary to form a mask anew for the ion implantation of the above-mentioned boron, and has further the effectiveness that simplification of a production process can be attained.
[0165] Moreover, the laminating of the polycrystalline silicon film and the silicon nitride is carried out to this order on the silicon substrate by which silicon oxide was formed in the front face. The process which forms a mask, and the process which oxidizes the above-mentioned silicon substrate thermally using the above-mentioned mask, The process which forms in the above-mentioned mask side face the sidewall which consists of a resist, Since the process which carries out the ion implantation of the impurity to the interior of the above-mentioned silicon substrate by using the above-mentioned sidewall as a mask, and the process which removes the above-mentioned sidewall by etching are provided High impurity concentration of the channel cut field located near the center of the component isolation region [directly under] of the above-mentioned component isolation region concerned can be made high, therefore it has the effectiveness that a semiconductor device with a low junction capacitance can be formed.
[0166] Moreover, the laminating of the polycrystalline silicon film and the silicon nitride is carried out to this order on the silicon substrate by which silicon oxide was formed in the front face. The process which forms a mask, and the process which forms in the side face of the above-mentioned mask the sidewall which consists of a resist, The process which carries out the ion implantation of the impurity to the interior of the above-mentioned silicon substrate by using the above-mentioned sidewall as a mask, Since the process which removes the above-mentioned sidewall by etching, and the process which oxidizes the above-mentioned silicon substrate thermally using the mask which consists of the above-mentioned polycrystalline silicon film and a silicon nitride are provided High impurity concentration of the channel cut field located near the center of the component isolation region [directly under] of the above-mentioned component isolation region concerned can be made high, therefore it has the effectiveness that

a semiconductor device with a low junction capacitance can be formed.

[Translation done.]

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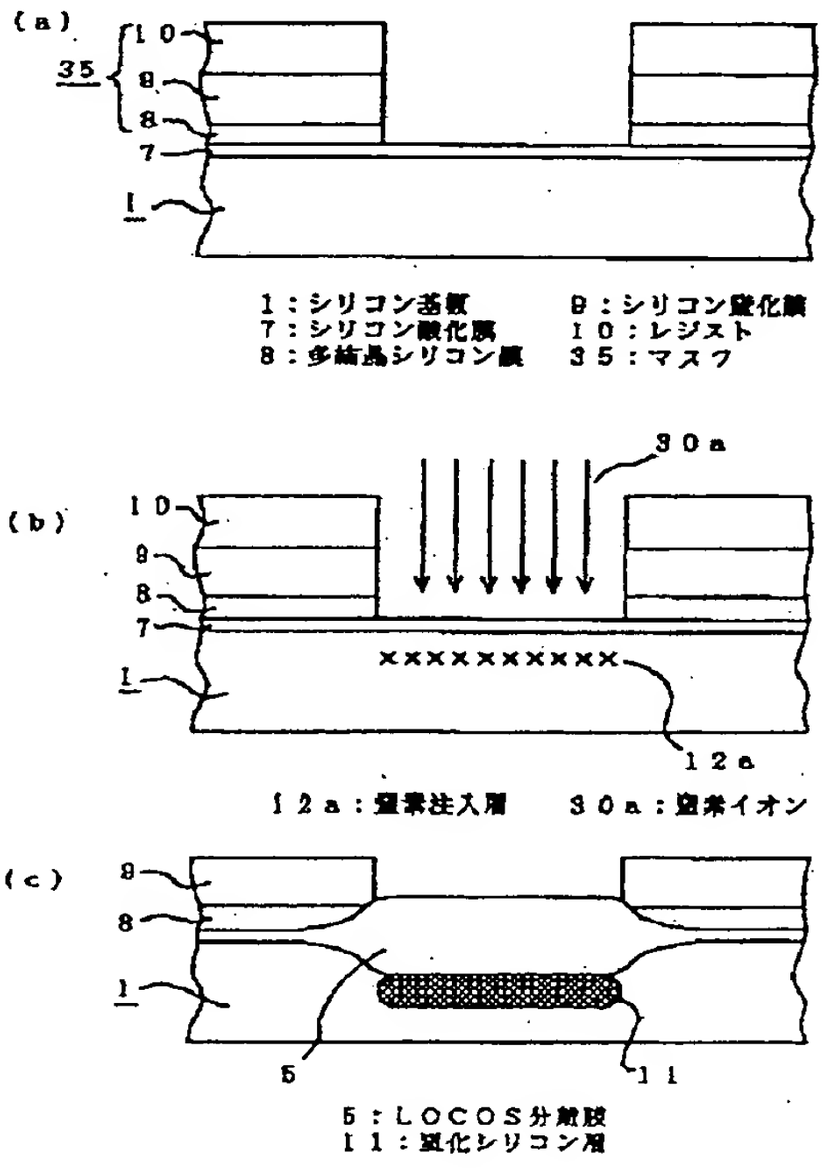
(54)【発明の名称】半導体装置及びその製造方法

(57)【要約】
【課題】　分離性能が良好であり、かつ接合容量が低減された半導体装置を得る。
【解決手段】　表面にシリコン酸化膜７が形成されているシリコン基板１上に、多結晶シリコン膜８、シリコン窒化膜９及びレジスト１０をこの順に積層して、マスク３５を形成する。このマスク３５を用いて、上記シリコン基板１に窒素イオン３０ａを注入して窒素注入層１２ａを形成する。上記マスク３５の一部であるレジスト１０を除去し、このレジスト１０が除去されたマスク３５を用いて、上記シリコン基板１を熱酸化することにより、上記シリコン基板１表面にＬＯＣＯＳ分離膜５を形成し、このＬＯＣＯＳ分離膜５の下に窒化シリコン層１１を形成する。



1

【特許請求の範囲】

【請求項１】　シリコン基板の表面上に形成されたマスクを用いた当該シリコン基板の酸化により、上記シリコン基板表面に形成された素子分離層と、

上記マスクを用いた上記シリコン基板への窒素のイオン注入により、上記素子分離層の下面近傍に形成された窒素含有層とを備えた半導体装置。

【請求項２】　窒素含有層は、素子分離層の下に形成された窒化シリコン層であることを特徴とする請求項１記載の半導体装置。

【請求項３】　窒素含有層は、素子分離層の下面を囲うような形状に形成されていることを特徴とする請求項１又は請求項２記載の半導体装置。

【請求項４】　窒素含有層は、素子分離層の内部に形成された窒化酸化シリコン層であることを特徴とする請求項１記載の半導体装置。

【請求項５】　半導体基板表面に形成された素子分離層を備え、

上記半導体基板表面の内、当該素子分離層が形成されている部分の近傍であり、かつ上記素子分離層が形成されていない部分を、当該素子分離層内部にまで延長した面を基準面として、上記素子分離層が、上記基準面に対する垂直断面における幅が異なる複数の領域を有するとともに、その幅に関係なく厚さがほぼ一定であることを特徴とする半導体装置。

【請求項６】　半導体基板表面に形成された素子分離層を備え、

上記半導体基板表面の内、当該素子分離層が形成されている部分の近傍であり、かつ上記素子分離層が形成されていない部分を、当該素子分離層内部にまで延長した面を基準面として、上記素子分離層が、上記基準面に対する垂直断面における幅が異なる複数の領域を有するとともに、その幅に関係なく上記基準面より上の部分の厚さがほぼ一定であることを特徴とする半導体装置。

【請求項７】　半導体基板の表面に形成された素子分離層と、

上記半導体基板の素子分離層が形成されている面の、上記素子分離層に囲まれた領域に形成されるとともに、側面が上記素子分離層に接している拡散領域とを備え、

上記半導体基板表面の内、当該素子分離層が形成されている部分の近傍であり、かつ上記素子分離層が形成されていない部分を、当該素子分離層内部にまで延長した面を基準面として、上記素子分離層は、この基準面に対する垂直断面において、当該垂直断面おける上記基準面より下の部分の厚さがほぼ一定であり、

上記拡散領域は、上記素子分離層に接している側面のほとんどが当該素子分離層に接していることを特徴とする半導体装置。

【請求項８】　表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜、シリコン窒化膜及びレジストをこの順に積層して、マスクを形成する工程と、

2

上記マスクを用いて、上記シリコン基板に窒素をイオン注入する工程と、

上記マスクの一部であるレジストを除去する工程と、

上記シリコン基板を上記レジストを除去したマスクを用いて熱酸化する工程とを含む半導体装置の製造方法。

【請求項９】　イオン注入は、斜め回転イオン注入によることを特徴とする請求項８記載の半導体装置の製造方法。

【請求項１０】　表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜及びシリコン窒化膜をこの順に積層して、マスクを形成する工程と、

上記シリコン基板を上記マスクを用いて熱酸化する工程と、

上記マスクを用いて、上記シリコン基板に窒素をイオン注入する工程とを含む半導体装置の製造方法。

【請求項１１】　マスクは、イオン注入される窒素が当該マスクを通過することを阻止するような厚さに形成されていることを特徴とする請求項１０記載の半導体装置の製造方法。

【請求項１２】　半導体基板の表面上にマスクを形成する工程と、

上記半導体基板を上記マスクを用いて熱酸化することにより、素子分離層を形成する工程と、

上記マスクを用いて、上記素子分離層をドライエッチングする工程とを含む半導体装置の製造方法。

【請求項１３】　半導体基板の表面上にマスクを形成する工程と、

上記半導体基板を上記マスクを用いて熱酸化することにより、素子分離層を形成する工程と、

上記半導体基板上に絶縁膜を形成する工程と、

上記絶縁膜を平坦化する工程と、

上記マスクの上端の一部が露出するまで、上記平坦化した絶縁膜を除去する工程と、

上記マスクを除去する工程とを含む半導体装置の製造方法。

【請求項１４】　表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜及びシリコン窒化膜をこの順に積層して、マスクを形成する工程と、

上記マスクを用いて、上記シリコン基板に酸素を斜め回転イオン注入する工程と、

上記シリコン基板を上記マスクを用いて熱酸化する工程とを含む半導体装置の製造方法。

【請求項１５】　シリコン基板の一主面に素子分離層を形成する工程と、

上記シリコン基板の一主面にリンを斜め回転イオン注入することにより、チャネルカット領域を形成する工程とを含む半導体装置の製造方法。

【請求項１６】　シリコン基板の一主面に、窒化酸化シ

リコン層を有する素子分離層を形成する工程と、
上記シリコン基板の一主面にボロンを斜め回転イオン注入することにより、チャネルカット領域を形成する工程とを含む半導体装置の製造方法。
【請求項１７】　チャネルカット領域を形成する工程は、注入されたリン又はボロンをアニール処理により再拡散させる工程を含むことを特徴とする請求項１５又は請求項１６記載の半導体装置の製造方法。
【請求項１８】　表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜及びシリコン窒化膜をこの順に積層して、マスクを形成する工程と、
上記シリコン基板を上記マスクを用いて熱酸化する工程と、
上記マスク側面にレジストからなるサイドウォールを形成する工程と、
上記サイドウォールをマスクとして、上記シリコン基板内部にイオン注入する工程と、
上記サイドウォールをエッチングにより除去する工程とを含む半導体装置の製造方法。
【請求項１９】　表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜及びシリコン窒化膜をこの順に積層して、マスクを形成する工程と、
上記マスクの側面にレジストからなるサイドウォールを形成する工程と、
上記サイドウォールをマスクとして、上記シリコン基板内部にイオン注入する工程と、
上記サイドウォールをエッチングにより除去する工程と、
上記多結晶シリコン膜及びシリコン窒化膜からなるマスクを用いて、上記シリコン基板を熱酸化する工程とを含む半導体装置の製造方法。
【請求項２０】　サイドウォールは、レジストに代わり、エッチングに対する選択比がシリコン酸化膜及びシリコン窒化膜よりも高い材質により形成することを特徴とする請求項１８又は請求項１９記載の半導体装置の製造方法。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】この発明は半導体装置の構造及びその製造方法に関するもので、特に複数の素子形成領域間の電気的な分離を行うための技術である、ＬＯＣＯＳ（ＬｏｃａｌＯｘｉｄａｔｉｏｎ　ｏｆ　Ｓｉｌｉｃｏｎ）に関するものである。
【０００２】
【従来の技術】従来、半導体集積回路の素子分離に用いられる分離酸化膜の形成方法として、ＬＯＣＯＳ（Ｌｏｃａｌ　Ｏｘｉｄａｔｉｏｎ　ｏｆ　Ｓｉｌｉｃｏｎ）が広く用いられてきた。しかし、半導体素子の微細化に伴い、上記ＬＯＣＯＳを用いた場合には、必要以上に横方向の酸化が進みバーズビークが発生することで、素子

形成領域の面積を余分に占有してしまい、その結果、半導体回路の集積化を拒む要因となっていた。そこで近年、このバーズビーク長を抑制するため、シリコン酸化膜とシリコン窒化膜との間に多結晶シリコン膜を挟んだ構造のマスクを用いた、Ｐｏｌｙ－Ｓｉ　ｂｕｆｆｅｒｅｄ　ＬＯＣＯＳ（以下、ＰＢＬと呼ぶ。）が用いられるようになってきている。
【０００３】以下に、ＰＢＬを用いてシリコン基板表面に形成された分離酸化膜と、そのシリコン基板に従来の製造方法を用いて形成された不純物領域とを備えた半導体装置の構造について、図２４及び図２５を用いて説明する。
【０００４】図２４は従来の半導体装置の構造を示す要部断面図であり、図２４において、１はシリコン基板、２はシリコン基板１の１主面に形成されたウェル領域、３はシリコン基板１の主面の上記ウェル領域２よりも浅い部分に形成されたチャネルカット領域、４はシリコン基板１の表面近傍の素子形成領域６に形成されたチャネルドープ領域、５は素子形成領域６の周囲を囲むように形成され、複数の素子形成領域６のそれぞれを電気的に分離する、例えば約４０００Åの膜厚を有する分離酸化膜（ＬＯＣＯＳ分離膜）である。
【０００５】図２５は従来の半導体装置の製造方法を工程順に示す要部断面図である。まず、図２５（ａ）に示すように、シリコン基板１表面を酸化することにより、例えば５０～５００Å程度の膜厚のシリコン酸化膜７を形成し、このシリコン酸化膜７上に例えば１００～１０００Å程度の膜厚の多結晶シリコン膜８ａ、及び、例えば５００～４０００Å程度の膜厚を有し、組成がＳｉ，Ｎ，であるシリコン窒化膜９ａを、この順に堆積する。ここで、シリコン酸化膜７は、ＣＶＤ法により形成しても良い。
【０００６】次に、図２５（ｂ）に示すように、シリコン基板１上にレジストを塗布し、通常の写真製版技術を用いて、当該レジストをパターニングするとともに、パターニングされたレジスト１０を用いて、上記シリコン窒化膜９ａ、多結晶シリコン膜８ａを順次エッチングして、シリコン窒化膜９及び多結晶シリコン膜８から成るマスクを形成する。。
【０００７】次に、図２５（ｃ）に示すように、レジスト１０を除去し、多結晶シリコン膜８及びシリコン窒化膜９からなるマスクを用いてシリコン基板１を熱酸化し、ＬＯＣＯＳ分離膜である分離酸化膜５を形成する。その後、多結晶シリコン膜８及びシリコン窒化膜９をエッチングにより除去する。
【０００８】次に、図２５（ｄ）に示すように、ウェル領域２を形成するための不純物２７のイオン注入（ウェル注入）を行い、ウェル領域２となる不純物領域２ａをシリコン基板１に形成する。ここで、注入エネルギーは、Ｐ型ウェル形成の場合とＮ型ウェル形成の場合と

5

で、又、製造プロセスの世代間で、それぞれ異なるエネルギーを用いるが、具体的には、例えば１００～２００ｋｅＶ程度の高エネルギーを用いる。

【０００９】次に、図２５（ｅ）に示すように、チャネルカット領域３を形成するための不純物２８のイオン注入（チャネルカット注入）を行い、チャネルカット領域３となる不純物領域３ａを形成する。ここで、注入エネルギーは、具体的には、１００～１０００ｋｅＶ程度のエネルギーを用いる。このチャネルカット注入は、複数の素子形成領域６のそれぞれを電気的に分離するために、分離酸化膜５の直下に不純物領域３ａが形成されるように、ウェル注入と同じ導電型の不純物を注入するものである。

【００１０】次に、図２５（ｆ）に示すように、チャネルドープ領域４を形成するための不純物２９のイオン注入（チャネルドープ注入）を行い、チャネルドープ領域４となる不純物領域４ａを形成する。ここで、注入エネルギーは、具体的には、５～１００ｋｅＶ程度のエネルギーを用いる。このチャネルドープ注入は、素子形成領域６に形成されるＭＯＳトランジスタなどのしきい値電圧を制御するために、シリコン基板１の表面近くに注入するものである。

【００１１】その後、アニール処理などの工程を経て、図２４にて示した半導体装置を得る。

【００１２】

【発明が解決しようとする課題】しかるに、このようにされた半導体記憶装置においては、チャネルカット注入における注入量が少ないと、素子形成領域６に形成されるソース・ドレイン領域にかかるバイアスの条件によっては、パンチスルー効果等により素子分離が不能となってしまうという問題があった。一方、このチャネルカット注入における注入量を多くすると、チャネルカット領域３と、素子形成領域６に形成されるソース・ドレイン領域との接合容量が増加するという問題もあった。

【００１３】この発明は上記した点に鑑みてなされたものであり、分離性能が良好であるとともに、接合容量の増加しない半導体装置を提供することを目的とするものである。

【００１４】

【課題を解決するための手段】この発明に係る半導体装置は、シリコン基板の表面上に形成されたマスクを用いた当該シリコン基板の酸化により、上記シリコン基板表面に形成された素子分離層と、上記マスクを用いた上記シリコン基板への窒素のイオン注入により、上記素子分離層の下面近傍に形成された窒素含有層とを設けたものである。

【００１５】又、上記窒素含有層は、素子分離層の下に形成された窒化シリコン層であることを特徴とするものである。

【００１６】又、上記窒素含有層は、素子分離層の下面

6

を囲うような形状に形成されていることを特徴とするものである。

【００１７】又、上記窒素含有層は、素子分離層の内部に形成された窒化酸化シリコン層であることを特徴とするものである。

【００１８】又、半導体基板表面に形成された素子分離層を備え、上記半導体基板表面の内、当該素子分離層が形成されている部分の近傍であり、かつ上記素子分離層が形成されていない部分を、当該素子分離層内部にまで延長した面を基準面として、上記素子分離層が、上記基準面に対する垂直断面における幅が異なる複数の領域を有するとともに、その幅に関係なく厚さがほぼ一定であることを特徴とするものである。

【００１９】又、半導体基板表面に形成された素子分離層を備え、上記半導体基板表面の内、当該素子分離層が形成されている部分の近傍であり、かつ上記素子分離層が形成されていない部分を、当該素子分離層内部にまで延長した面を基準面として、上記素子分離層が、上記基準面に対する垂直断面における幅が異なる複数の領域を有するとともに、その幅に関係なく上記基準面より上の部分の厚さがほぼ一定であることを特徴とするものである。

【００２０】又、半導体基板の表面に形成された素子分離層と、上記半導体基板の素子分離層が形成されている面の、上記素子分離層に囲まれた領域に形成されるとともに、側面が上記素子分離層に接している拡散領域とを備え、上記半導体基板表面の内、当該素子分離層が形成されている部分の近傍であり、かつ上記素子分離層が形成されていない部分を、当該素子分離層内部にまで延長した面を基準面として、上記素子分離層は、この基準面に対する垂直断面において、当該垂直断面おける上記基準面より下の部分の厚さがほぼ一定であり、上記拡散領域は、上記素子分離層に接している側面のほとんどが当該素子分離層に接していることを特徴とするものである。

【００２１】この発明に係る半導体装置の製造方法は、表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜、シリコン窒化膜及びレジストをこの順に積層して、マスクを形成する工程と、上記マスクを用いて、上記シリコン基板に窒素をイオン注入する工程と、上記マスクの一部であるレジストを除去する工程と、上記シリコン基板を上記レジストを除去したマスクを用いて熱酸化する工程とを具備するものである。

【００２２】又、上記イオン注入は、斜め回転イオン注入によることを特徴とするものである。

【００２３】又、表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜及びシリコン窒化膜をこの順に積層して、マスクを形成する工程と、上記シリコン基板を上記マスクを用いて熱酸化する工程と、上記マスクを用いて、上記シリコン基板に窒素をイオン注

入する工程とを具備するものである。
【００２４】又、上記マスクは、イオン注入される窒素が当該マスクを通過することを阻止するような厚さに形成されていることを特徴とするものである。
【００２５】又、半導体基板の表面上にマスクを形成する工程と、上記半導体基板を上記マスクを用いて熱酸化することにより、素子分離層を形成する工程と、上記マスクを用いて、上記素子分離層をドライエッチングする工程とを具備するものである。
【００２６】又、半導体基板の表面上にマスクを形成する工程と、上記半導体基板を上記マスクを用いて熱酸化することにより、素子分離層を形成する工程と、上記半導体基板上に絶縁膜を形成する工程と、上記絶縁膜を平坦化する工程と、上記マスクの上端の一部が露出するまで、上記平坦化した絶縁膜を除去する工程と、上記マスクを除去する工程とを具備するものである。
【００２７】又、表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜及びシリコン窒化膜をこの順に積層して、マスクを形成する工程と、上記マスクを用いて、上記シリコン基板に酸素を斜め回転イオン注入する工程と、上記シリコン基板を上記マスクを用いて熱酸化する工程とを具備するものである。
【００２８】又、シリコン基板の一主面に素子分離層を形成する工程と、上記シリコン基板の一主面にリンを斜め回転イオン注入することにより、チャネルカット領域を形成する工程とを具備するものである。
【００２９】又、シリコン基板の一主面に、窒化酸化シリコン層を有する素子分離層を形成する工程と、上記シリコン基板の一主面にボロンを斜め回転イオン注入することにより、チャネルカット領域を形成する工程とを具備するものである。
【００３０】又、上記チャネルカット領域を形成する工程は、注入されたリン又はボロンをアニール処理により再拡散させる工程を含むことを特徴とするものである。
【００３１】又、表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜及びシリコン窒化膜をこの順に積層して、マスクを形成する工程と、上記シリコン基板を上記マスクを用いて熱酸化する工程と、上記マスク側面にレジストからなるサイドウォールを形成する工程と、上記サイドウォールをマスクとして、上記シリコン基板内部にイオン注入する工程と、上記サイドウォールをエッチングにより除去する工程とを具備するものである。
【００３２】又、表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜及びシリコン窒化膜をこの順に積層して、マスクを形成する工程と、上記マスクの側面にレジストからなるサイドウォールを形成する工程と、上記サイドウォールをマスクとして、上記シリコン基板内部にイオン注入する工程と、上記サイドウォールをエッチングにより除去する工程と、上記多結晶シリコン膜及びシリコン窒化膜からなるマスクを用いて、上記シリコン基板を熱酸化する工程とを具備するものである。
【００３３】又、上記サイドウォールは、レジストに代わり、エッチングに対する選択比がシリコン酸化膜及びシリコン窒化膜よりも高い材質により形成することを特徴とするものである。
【００３４】
【発明の実施の形態】
実施の形態１．以下に、この発明の実施の形態１について図１ないし図３に基づいて説明する。図１は、本発明の実施の形態１を示す要部断面図であり、図１において、１はシリコン基板であり、５はこのシリコン基板１表面に形成された素子分離層であるＬＯＣＯＳ分離膜である。１１は、このＬＯＣＯＳ分離膜５の下面近傍の当該下面の下に形成された窒化シリコン層である。
【００３５】つぎに、このように構成された半導体装置の製造方法について図２及び図３を用いて説明する。図２及び図３はそれぞれ本実施の形態１を工程順に示す要部断面図である。
【００３６】上記図１に示す半導体装置の１の製造方法を図２に示す。まず、図２（ａ）に示すように、表面にシリコン酸化膜７が形成されているシリコン基板１上に、多結晶シリコン膜８、シリコン窒化膜９及びレジスト１０をこの順に積層して、通常の写真製版技術を用い、マスク３５を形成する。
【００３７】次に、図２（ｂ）に示すように、レジスト１０の除去を行わずに、上記マスク３５を用いて、上記シリコン基板１に窒素イオン３０ａを注入して窒素注入層１２ａを形成する。ここで、窒素イオン３０ａの注入には、後の工程において形成されるＬＯＣＯＳ分離膜５の下面近傍の当該下面の下に、窒素注入層１２ａが形成されるようなエネルギーを用いることとする。又、ここで、上記半導体基板表面の内で、マスク３５に覆われている部分には、当該マスク３５が障壁となることにより、窒素イオン３０ａが注入されることはない。
【００３８】次に、図２（ｃ）に示すように、上記マスク３５の一部であるレジスト１０を除去し、このレジスト１０が除去されたマスク３５を用いて、上記シリコン基板１を熱酸化することにより、上記シリコン基板１表面にＬＯＣＯＳ分離膜５を形成する。その後、上記マスク３５をエッチングにより除去して、上記ＬＯＣＯＳ分離膜５の下面近傍の当該下面の下に窒化シリコン層１１を有する、図１に示す半導体装置を得る。
【００３９】上記図２に示す半導体装置の製造方法によれば、窒素イオン３０ａ注入用のマスク形成のための写真製版工程を改めて設ける必要がなく、そのため、図１に示す半導体装置の製造工程数を減らすことができ、しかも、ＬＯＣＯＳ分離膜５の形成のための熱酸化を行う前に、上記窒素イオン３０ａの注入を行っているので、

9

ＬＯＣＯＳ分離膜５の形成後に窒素イオンの注入を行う場合に比べて、高エネルギーの窒素イオン注入装置を必要とせず、半導体装置の製造コストを全体として低減することが可能となる。

【００４０】上記図１に示す半導体装置の他の製造方法を図３に示す。まず、図３（ａ）に示すように、表面にシリコン酸化膜７が形成されているシリコン基板１上に、多結晶シリコン膜８、シリコン窒化膜９及びレジスト１０をこの順に積層して、通常の写真製版技術を用いてレジスト１０をパターニングし、このパターニングされたレジスト１０をマスクとして多結晶シリコン膜８及びシリコン窒化膜９のエッチングを行う。

【００４１】次に、図３（ｂ）に示すように、上記エッチングされた多結晶シリコン膜８及びシリコン窒化膜９からなるマスク３６を用いて、上記シリコン基板１を熱酸化することにより、上記シリコン基板１表面のマスク３６の開口部にＬＯＣＯＳ分離膜５を形成する。

【００４２】次に、図３（ｃ）に示すように、上記マスク３６を用いて窒素イオン３０ｂを注入し、上記ＬＯＣＯＳ分離膜５の下面近傍の当該下面の下に窒素注入層１２ｂを形成する。ここで、マスク３６の厚さは、窒素イオン３０ｂが通過しないような厚さとなっている。。

【００４３】その後、上記マスク３６をエッチングにより除去して、上記ＬＯＣＯＳ分離膜５の下面近傍の当該下面の下に窒化シリコン層１１を有する、図１に示す半導体装置を得る。

【００４４】上記図３に示す半導体装置の製造方法によれば、窒素イオン３０ｂ注入用のマスク形成のための写真製版工程を改めて設ける必要がなく、そのため、図１に示す半導体装置の製造工程数を減らすことができる。

【００４５】しかも、ＬＯＣＯＳ分離膜５の形成後に、上記窒素イオン３０ｂの注入を行っているので、ＬＯＣＯＳ分離膜５の形成前に窒素イオンの注入を行う場合に比べ、当該ＬＯＣＯＳ分離膜５の形成のための高温の熱処理工程における注入窒素原子の再分布が起こらず、そのため、窒化シリコン層１１の膜厚、深さ及び窒素濃度などの制御が容易に行うことが可能となるという効果を有する。

【００４６】従来、ＬＯＣＯＳ分離膜５の下面の周囲に存在するチャネルカット領域を形成する不純物が、熱処理などによって、当該ＬＯＣＯＳ分離膜５の内部に拡散し吸収されることにより、その不純物濃度が低下し、そのために、パンチスルー現象などの分離耐圧の劣化が生ていた。特に、ＮチャネルＭＯＳトランジスタの素子分離領域においては、チャネルカット領域を形成する不純物であるボロンが、熱処理によりＬＯＣＯＳ分離膜５の内部に拡散し吸収され易い性質を有しているため、上記の傾向は顕著であった。

【００４７】しかし、本発明の実施の形態１に示す半導体装置によれば、ＬＯＣＯＳ分離膜５の下面近傍の当該

10

下面の下に窒化シリコン膜１１を形成したので、上記ボロンなどの不純物のＬＯＣＯＳ分離膜５の内部への拡散、吸収を抑制、防止でき、そのため、分離耐圧の劣化を防ぐことが可能となる。

【００４８】又、本発明の実施の形態１に示す半導体装置によれば、チャネルカット領域形成用のボロンなどの不純物を、当該不純物のＬＯＣＯＳ分離膜５の内部への拡散、吸収を見越して、予め、注入量を多くしておく必要がなく、そのため、ウェル領域全体としての不純物量を低下することができ、接合容量の低減が可能となる。

【００４９】又、素子分離領域の実効的な膜厚が、ＬＯＣＯＳ分離膜５の膜厚及び窒化シリコン層１１の膜厚を加えたものとなるので、このＬＯＣＯＳ分離膜５の上層に形成されるワード線などの配線の、配線容量を低減することも可能となる。

【００５０】実施の形態２．図４はこの発明の実施の形態２を示す要部断面図であり、実施の形態１に対して、ＬＯＣＯＳ分離膜５の下面近傍の当該下面の下に窒化シリコン層１１を備える代わりに、ＬＯＣＯＳ分離膜５の下面近傍の当該ＬＯＣＯＳ分離膜５の内部に窒化酸化シリコン層１３を備えている点で相違するだけであり、他の点については上記した実施の形態１と同様である。

【００５１】但し、当該半導体装置の１の製造方法として、実施の形態１においては、図２（ｂ）に示すように、窒素イオン３０ａの注入には、ＬＯＣＯＳ分離膜５の下面近傍の当該下面の下に窒素注入層１２ａが形成されるようなエネルギーを用いているのに対し、本実施の形態２においては、窒素イオン３０ａの注入エネルギーは、上記ＬＯＣＯＳ分離膜５の下面近傍の当該ＬＯＣＯＳ分離膜５内部に窒素注入層１２ａが形成されるようなエネルギーを用いる。

【００５２】本実施の形態２においても、上記図２に示される当該半導体装置の１の製造方法によれば、窒素イオン３０ａ注入用のマスク形成のための写真製版工程を改めて設ける必要がなく、そのため、当該半導体装置の製造工程数を減らすことができ、しかも、ＬＯＣＯＳ分離膜５の形成のための熱酸化を行う前に、上記窒素イオン３０ａの注入を行っているので、ＬＯＣＯＳ分離膜５の形成後に窒素イオンの注入を行う場合に比べて、高エネルギーの窒素イオン注入装置を必要とせず、半導体装置の製造コストを全体として低減することが可能となる。

【００５３】又、当該半導体装置の他の製造方法として、実施の形態１においては、図３（ｃ）に示すように、上記マスク３６を用いて窒素イオン３０ｂを注入し、上記ＬＯＣＯＳ分離膜５の下面近傍の当該下面の下に窒素注入層１２ｂを形成しているのに対し、本実施の形態２においては、上記ＬＯＣＯＳ分離膜５の下面近傍の当該ＬＯＣＯＳ分離膜５の内部に窒素注入層１２ｂを形成する。

【００５４】本実施の形態２においても、上記図３に示される当該半導体装置の他の製造方法によれば、窒素イオン3.０ｂ注入用のマスク形成のための写真製版工程を改めて設ける必要がなく、そのため、当該半導体装置の製造工程数を減らすことができる。

【００５５】しかも、ＬＯＣＯＳ分離膜５の形成後に、上記窒素イオン３０ｂの注入を行っているので、ＬＯＣＯＳ分離膜５の形成前に窒素イオンの注入を行う場合に比べ、当該ＬＯＣＯＳ分離膜５の形成のための高温の熱処理工程における注入窒素原子の再分布が起こらず、そのため、窒化酸化シリコン層１３の膜厚、深さ及び窒素濃度などの制御が容易に行うことが可能となるという効果を有する。

【００５６】本発明の実施の形態２に示す半導体装置によれば、ＬＯＣＯＳ分離膜５の下面近傍の当該ＬＯＣＯＳ分離膜５の内部に窒化酸化シリコン膜１３を形成したので、上記ボロンなどの不純物のＬＯＣＯＳ分離膜５の内部への拡散、吸収を抑制、防止でき、そのため、分離耐圧の劣化を防ぐことが可能となる。

【００５７】又、本発明の実施の形態２に示す半導体装置によれば、チャネルカット領域形成用のボロンなどの不純物を、当該不純物のＬＯＣＯＳ分離膜５の内部への拡散、吸収を見越して、予め、注入量を多くしておく必要がなく、そのため、ウェル領域全体としての不純物量を低下することができ、接合容量の低減が可能となる。

【００５８】又、本発明の実施の形態２に示す半導体装置によれば、ＬＯＣＯＳ分離膜５の下面の近傍に窒化酸化シリコン層１３が形成されており、この窒化酸化シリコン層１３中には酸素原子が含まれているので、シリコン基板１とこの窒化酸化シリコン層１３との膨張係数の差が小さく、そのため、シリコン基板１とＬＯＣＯＳ分離膜５との界面に生じるストレスによるリーク電流を小さく抑えることが可能となる。

【００５９】実施の形態３．図５はこの発明の実施の形態３を示す要部断面図であり、実施の形態１に対して、窒化シリコン層１１をＬＯＣＯＳ分離膜５の下面近傍の当該下面の下にのみ形成するに留まらず、窒化シリコン層１１をＬＯＣＯＳ分離膜５の下面を囲うように、つまり、バーズビーク領域の直下においても形成する点で相違するだけであり、他の点については上記した実施の形態１と同様である。

【００６０】但し、当該半導体装置の１の製造方法としては、上記図２にて示した製造方法を用い、上記図２（ｂ）に示した工程の代わりに、図６に示すように、窒素イオン３０ｃの注入を斜め回転イオン注入機を用いて行う工程を用いる。

【００６１】本実施の形態３においても、上記図２に示す当該半導体装置の製造方法によれば、斜め回転イオン注入される窒素イオン３０ｃの注入用のマスクを形成するために、写真製版工程を改めて設ける必要がなく、そのため、図５に示す半導体装置の製造工程数を減らすことができ、しかも、ＬＯＣＯＳ分離膜５の形成のための熱酸化を行う前に、上記窒素イオン３０ｃの注入を行っているので、ＬＯＣＯＳ分離膜５の形成後に窒素イオンの注入を行う場合に比べて、高エネルギーの窒素イオン注入装置を必要とせず、半導体装置の製造コストを全体として低減することが可能となる。

【００６２】本発明の実施の形態３に示す半導体装置によれば、ＬＯＣＯＳ分離膜５の下面を囲むように窒化シリコン膜１１を形成したので、ボロンなどの不純物のＬＯＣＯＳ分離膜５の内部への拡散、吸収を抑制、防止でき、そのため、分離耐圧の劣化を防ぐことが可能となる。特に、バーズビーク直下における不純物のＬＯＣＯＳ分離膜５の内部への拡散、吸収を抑制、防止できる効果がある。

【００６３】又、本発明の実施の形態３に示す半導体装置によれば、チャネルカット領域形成用のボロンなどの不純物を、当該不純物のＬＯＣＯＳ分離膜５の内部への拡散、吸収を見越して、予め、注入量を多くしておく必要がなく、そのため、ウェル領域全体としての不純物量を低下することができ、接合容量の低減が可能となる。

【００６４】又、本発明の実施の形態３に示す半導体装置によれば、その製造時において、マスク３５と窒素注入層１２ｃに挟まれた領域は、この上下の窒素含有層からのストレスにより、ＬＯＣＯＳ分離膜５の形成時における熱酸化工程においてバーズビークが形成されにくくなり、そのため、素子の高集積化が可能となる。

【００６５】実施の形態４．図７は、従来の半導体装置を示す要部断面図であり、図７において、１はシリコン基板であり、５ａ、５ｂはこのシリコン基板１表面に形成された異なる分離幅Ｗ１、Ｗ２を有する素子分離層であるＬＯＣＯＳ分離膜である。１４はＬＯＣＯＳ分離膜５ａに対応のチャネルカット領域であり、当該ＬＯＣＯＳ分離膜５ａの下に形成されるようにエネルギーを調整したイオン注入により形成されたものである。一方、１５はＬＯＣＯＳ分離膜５ｂに対応するチャネルカット領域であり、当該ＬＯＣＯＳ分離膜５ｂの下に形成されるようにエネルギーを調整したイオン注入により形成されている。

【００６６】上記従来の半導体装置においては、ＬＯＣＯＳ分離膜５ａ、５ｂのそれぞれの幅に対応してその膜厚が異なる。具体的には、幅の広いＬＯＣＯＳ分離膜５ａでは、その膜厚は、幅の狭いＬＯＣＯＳ分離膜５ｂに比べて厚くなる。この膜厚の差に対応してチャネルカット領域を形成するために、１回のチャネルカット注入で済ますのではなく、チャネルカット注入を膜厚の異なるＬＯＣＯＳ分離膜５ａ及び５ｂのそれぞれに対応した最適な注入エネルギーを用いて、複数回行うこととすると、それぞれのＬＯＣＯＳ分離膜５ａ、５ｂにおいて分離耐圧が劣化することは免れる。

【００６７】しかし、この場合においては、幅の狭いＬＯＣＯＳ分離膜５ｂの下においては、複数回のチャネルカット注入による不純物の累積が起こり、不純物濃度が大きくなり、そのため、接合容量が大きくなってしまうという問題が起こっていた。

【００６８】そこで、上記問題を解決するための本発明の実施の形態４を以下に示すこととする。

【００６９】この発明の実施の形態４について、図８ないし図１１に基づいて説明する。図８は、本発明の実施の形態４を示す１の要部断面図であり、図８において、１はシリコン基板であり、５ｃ、５ｄはこのシリコン基板１表面に形成された異なる分離幅Ｗ１、Ｗ２を有する素子分離層であるＬＯＣＯＳ分離膜である。４０は、シリコン基板１表面の内、上記ＬＯＣＯＳ分離膜５ｃ、５ｄが形成されている部分の近傍であって、しかも、当該ＬＯＣＯＳ分離膜５ｃ、５ｄが形成されていない部分を、当該ＬＯＣＯＳ分離層５ｃ、５ｄの内部にまで延長した面（以下、基準面と呼ぶ。）である。

【００７０】ｘ１、ｘ２はＬＯＣＯＳ分離膜５ｃ、５ｄの基準面４０より上の部分の厚さ、ｙ１、ｙ２はＬＯＣＯＳ分離膜５ｃ、５ｄの基準面４０より下の部分の厚さであり、本実施の形態４においては、上記ｘ１、ｘ２はほぼ等しい値を有する。１６ａはＬＯＣＯＳ分離膜５ｃ及び５ｄに対応のチャネルカット領域であり、当該ＬＯＣＯＳ分離膜５ｃ、５ｄの下に形成されるように、エネルギーを調整した１回のイオン注入により形成されたものである。

【００７１】図８にて示す半導体装置においては、ＬＯＣＯＳ分離膜５ｃ。５ｄの基準面４０より上の部分の厚さｘ１、ｘ２はほぼ等しい値を有するので、両ＬＯＣＯＳ分離膜５ｃ。５ｄの上層に形成されるワード線などの配線の寸法ばらつきを抑えることが可能となる。

【００７２】つぎに、このように構成された半導体装置の製造方法について図９を用いて説明する。図９は図８に示される半導体装置の製造方法をを工程順に示す要部断面図である。

【００７３】まず、図９（ａ）に示すように、従来の半導体装置の製造方法と同様に、表面にシリコン酸化膜７が形成されているシリコン基板１上に、多結晶シリコン膜８、シリコン窒化膜９及びレジスト１０をこの順に積層して、通常の写真製版技術を用いてレジスト１０をパターニングし、このパターニングされたレジスト１０をマスクとして多結晶シリコン膜８及びシリコン窒化膜９のエッチングを行い、上記エッチングされた多結晶シリコン膜８及びシリコン窒化膜９からなるマスク３７を用いて、上記シリコン基板１を熱酸化することにより、上記シリコン基板１表面のマスク３７の開口部に、異なる分離幅Ｗ１、Ｗ２を有するＬＯＣＯＳ分離膜５ａ、５ｂを形成する。

【００７４】次に、図９（ｂ）に示すように、上記マスク３７を用いたドライエッチングにより、上記ＬＯＣＯＳ分離膜５ａ、５ｂを基準面４０より上の部分の厚さｘ１、ｘ２の値を等しくすることにより、ＬＯＣＯＳ分離膜５ｃ、５ｄを形成する。

【００７５】ここで、上記図９（ｂ）に示す工程においては、ＬＯＣＯＳ分離膜５ｃ、５ｄのそれぞれの幅の違いにより、エッチング時におけるマイクロローデイング効果が異なり、そのため、それぞれのＬＯＣＯＳ分離膜５ｃ、５ｄに対するエッチングレートが異なることとなり、基準面４０より上の部分の厚さｘ１、ｘ２の値をほぼ等しくすることが可能となる。

【００７６】具体的には、例えば、Ｗ２の値が０．２μｍ、多結晶シリコン膜８の膜厚が１０００Å、シリコン窒化膜９の膜厚が４０００ÅであるＬＯＣＯＳ分離膜５ｂにおいては、マスク３７の開口部のアスペクト比が約２．５となり、マイクロローデイング効果によるエッチングレートの低下が無視できないのに対し、Ｗ１の値が大きいＬＯＣＯＳ分離膜５ａにおいては、マイクロローデイング効果によるエッチングレートの低下は無視できる。

【００７７】そのため、ＬＯＣＯＳ分離膜５ｃのエッチングレートに対して、ＬＯＣＯＳ分離膜５ｄのエッチングレートは小さくなり、基準面４０より上の部分の厚さｘ１、ｘ２の値をほぼ等しくすることが可能となるのである。

【００７８】その後、上記マスク３７をエッチングにより除去し、両ＬＯＣＯＳ分離膜５ｃ、５ｄの下に形成されるように、エネルギーを調整した１回のイオン注入によりチャネルカット領域１６ａを形成することにより、図８に示す半導体装置を得る。

【００７９】図１０は、本発明の実施の形態４を示す他の要部断面図であり、図１０において、１はシリコン基板であり、５ｅ、５ｆはこのシリコン基板１表面に形成された異なる分離幅Ｗ１、Ｗ２を有する素子分離層であるＬＯＣＯＳ分離膜である。

【００８０】ｚ１、ｚ２はＬＯＣＯＳ分離膜５ｅ、５ｆの膜厚であり、本実施の形態４においては、上記ｚ１、ｚ２はほぼ等しい値を有する。１６ｂはＬＯＣＯＳ分離膜５ｅ及び５ｆに対応のチャネルカット領域であり、当該ＬＯＣＯＳ分離膜５ｅ、５ｆの下に形成されるように、エネルギーを調整した１回のイオン注入により形成されたものである。

【００８１】つぎに、このように構成された半導体装置の製造方法について図１１を用いて説明する。図１１は図１０に示される半導体装置の製造方法を工程順に示す要部断面図である。

【００８２】まず、図１１（ａ）に示すように、上記図９（ａ）と同様に、表面にシリコン酸化膜７が形成されているシリコン基板１上に、多結晶シリコン膜８、シリコン窒化膜９及びレジスト１０をこの順に積層して、通

常の写真製版技術を用いてレジスト１０をパターニングし、このパターニングされたレジスト１０をマスクとして多結晶シリコン膜８及びシリコン窒化膜９のエッチングを行い、上記エッチングされた多結晶シリコン膜８及びシリコン窒化膜９からなるマスク３７を用いて、上記シリコン基板１を熱酸化することにより、上記シリコン基板１表面のマスク３７の開口部に、異なる分離幅Ｗ１、Ｗ２を有するＬＯＣＯＳ分離膜５ａ、５ｂを形成する。

【００８３】次に、図１１（ｂ）に示すように、上記マスク３７を用いたドライエッチングにより、上記ＬＯＣＯＳ分離膜５ａ、５ｂの膜厚ｚ１、ｚ２の値を等しくすることにより、ＬＯＣＯＳ分離膜５ｅ、５ｆを形成する。

【００８４】ここで、膜厚ｚ１、ｚ２の値を等しくすることが可能な理由は、上記のマイクローデイング効果によるエッチングレートの違いに起因し、ここで、上記図９（ｂ）にて示された状態よりも、さらにエッチングを加えることにより、膜厚ｚ１、ｚ２の値をほぼ等しくすることが可能となる。

【００８５】その後、上記マスク３７をエッチングにより除去し、両ＬＯＣＯＳ分離膜５ｅ、５ｆの下に形成されるように、エネルギーを調整した１回のイオン注入によりチャネルカット領域１６ｂを形成することにより、図１０に示す半導体装置を得る。

【００８６】本発明の実施の形態４に示す半導体装置によれば、ＬＯＣＯＳ分離膜５ｃ、５ｄ又は５ｅ、５ｆの膜厚の差を小さくできるため、１回の最適な注入エネルギーを用いたチャネルカット注入により、有効な分離耐圧を有するチャネルカット領域を形成することが可能となる。

【００８７】そのため、複数回のチャネルカット注入を行う必要がなくなり、幅の狭いＬＯＣＯＳ分離膜５ｄ又は５ｆの下のチャネルカット領域においても、不純物の累積が起こるという問題がなくなり、結果として、接合容量を小さく抑えることが可能となる。

【００８８】実施の形態５．実施の形態４にて示した問題点に対応するための、本発明の実施の形態５を以下に説明する。

【００８９】この発明の実施の形態５について、図１２及び図１３に基づいて説明する。図１２は、本発明の実施の形態５を示す要部断面図であり、図１２において、１はシリコン基板であり、５ａ、５ｂはこのシリコン基板１表面に形成された異なる分離幅Ｗ１、Ｗ２を有する素子分離層であるＬＯＣＯＳ分離膜である。１７ａ、１７ｂはそれぞれＬＯＣＯＳ分離膜５ａ、５ｂ上に形成されたＢＰＳＧ膜であり、５ｇ、５ｈはＬＯＣＯＳ分離膜５ａ又は５ｂとその上のＢＰＳＧ膜１７ａ又は１７ｂより形成される素子分離層である。４０は基準面である。

【００９０】ｔ１、ｔ２は素子分離層５ｇ、５ｈの基準面４０より上の部分の厚さであり、本実施の形態５においては、上記ｔ１、ｔ２はほぼ等しい値を有する。１６ｃは素子分離層５ｇ及び５ｈに対応のチャネルカット領域であり、当該素子分離層５ｇ、５ｈの下に形成されるように、エネルギーを調整した１回のイオン注入により形成されたものである。

【００９１】つぎに、このように構成された半導体装置の製造方法について図１３を用いて説明する。図１３は本実施の形態５を工程順に示す要部断面図である。

【００９２】まず、図１３（ａ）に示すように、従来の半導体装置の製造方法と同様に、表面にシリコン酸化膜７が形成されているシリコン基板１上に、多結晶シリコン膜８、シリコン窒化膜９及びレジスト１０をこの順に積層して、通常の写真製版技術を用いてレジスト１０をパターニングし、このパターニングされたレジスト１０をマスクとして多結晶シリコン膜８及びシリコン窒化膜９のエッチングを行い、上記エッチングされた多結晶シリコン膜８及びシリコン窒化膜９からなるマスク３７を用いて、上記シリコン基板１を熱酸化することにより、上記シリコン基板１表面のマスク３７の開口部に、異なる分離幅Ｗ１、Ｗ２を有するＬＯＣＯＳ分離膜５ａ、５ｂを形成する。

【００９３】次に、図１３（ｂ）に示すように、例えばＢＰＳＧ膜からなる絶縁膜１７をシリコン基板１上に全面に堆積する。ここで、堆積する絶縁膜は上記ＢＰＳＧ膜に限らず、後の工程において、ＣＭＰ法などにより平坦化が可能であるものであればよい。

【００９４】次に、図１３（ｃ）に示すように、ＢＰＳＧ膜１７をＣＭＰ法により平坦化して、マスク３７の上端の１部が露出するまで除去する。ここで、ＢＰＳＧ膜１７の平坦化とマスク３７の上端の１部を露出させるための方法として、ＣＭＰ法の代わりに、Ｏ２ドライリフロー処理及びＢＰＳＧ膜１７のエッチバックを組み合わせる方法を用いても良い。

【００９５】その後、Ｈ，ＰＯ，等を用いた処理を行い、マスク３７を構成するシリコン窒化膜９、及びその上に若干残っていたＢＰＳＧ膜１７を除去し、続いて、多結晶シリコン膜８をエッチングにより除去し、最後に、両素子分離層５ｅ、５ｆの下に形成されるように、エネルギーを調整した１回のイオン注入によりチャネルカット領域１６ｃを形成することにより、図１２に示す半導体装置を得る。

【００９６】本発明の実施の形態５に示す半導体装置によれば、素子分離層５ｇ、５ｈの膜厚の差を小さくできるため、１回の最適な注入エネルギーを用いたチャネルカット注入により、有効な分離耐圧を有するチャネルカット領域を形成することが可能となる。

【００９７】そのため、複数回のチャネルカット注入を行う必要がなくなり、幅の狭いＬＯＣＯＳ分離膜５ｂの下のチャネルカット領域においても、不純物の累積が起

こるという問題がなくなり、結果として、接合容量を小さく抑えることが可能となる。

【００９８】又、本発明の実施の形態５に示す半導体装置によれば、マスク３７の膜厚が薄い場合、及び、分離幅Ｗ１、Ｗ２が比較的広い場合などの、マイクローデイング効果によるエッチングレートの違いが起こらない場合においても、実施の形態４と異なり、素子分離層５ｇ、５ｈの膜厚の差を小さくできるため、上記の効果を有するという特徴がある。

【００９９】実施の形態６．図１４は、従来の半導体装置を示す要部断面図であり、図１４において、１はシリコン基板、２はＰ型ウェル領域、５はシリコン基板１表面に形成された素子分離層であるＬＯＣＯＳ分離膜である。１８はＬＯＣＯＳ分離膜５に囲まれた素子形成領域中に形成されているＮ型拡散領域であり、１９は上記ＬＯＣＯＳ分離膜５に接する側の拡散領域１８の側面を表す。

【０１００】上記従来の半導体装置においては、Ｎ型拡散領域の側面１９において、Ｐ型ウェル２との接触面積が大きく、そのため、接合容量が大きくなってしまうという問題が起こっていた。

【０１０１】そこで、上記問題を解決するための本発明の実施の形態６を以下に示すこととする。

【０１０２】この発明の実施の形態６について、図１５及び図１６に基づいて説明する。図１５は、本発明の実施の形態６を示す要部断面図であり、図１５において、１はシリコン基板、２は例えばＰ型を示すウェル領域、２０はシリコン基板１表面に形成された素子分離層であるＬＯＣＯＳ分離膜である。４０は、シリコン基板１表面の内、上記ＬＯＣＯＳ分離膜２０が形成されている部分の近傍であって、しかも、当該ＬＯＣＯＳ分離膜２０が形成されていない部分を、当該ＬＯＣＯＳ分離層２０の内部にまで延長した面である基準面、１８はＬＯＣＯＳ分離膜２０に囲まれた素子形成領域中に形成されている例えばＮ型を示す拡散領域であり、１９は上記ＬＯＣＯＳ分離膜２０に接する側の当該拡散領域１８の側面を表す。

【０１０３】Ｔ１、Ｔ２はどちらもＬＯＣＯＳ分離膜２０の基準面４０より下の部分の厚さであり、特にＴ１はＬＯＣＯＳ分離膜２０の中央付近での上記厚さを表し、Ｔ２はＬＯＣＯＳ分離膜２０のバーズビーク付近での上記厚さを表しており、本実施の形態６においては、上記Ｔ１、Ｔ２はほぼ等しい値を有する。又、本実施の形態６においては、拡散領域の側面１９のほとんどが、ＬＯＣＯＳ分離膜２０に接しているという特徴を有する。

【０１０４】つぎに、このように構成された半導体装置の製造方法について図１６を用いて説明する。図１６は図１５に示される半導体装置の製造方法をを工程順に示す要部断面図である。

【０１０５】まず、図１６（ａ）に示すように、従来の

半導体装置の製造方法と同様に、表面にシリコン酸化膜７が形成されているシリコン基板１上に、多結晶シリコン膜８、シリコン窒化膜９及びレジストをこの順に積層して、通常の写真製版技術を用いてレジストをパターニングし、このパターニングされたレジストをマスクとして多結晶シリコン膜８及びシリコン窒化膜９のエッチングを行い、上記エッチングされた多結晶シリコン膜８及びシリコン窒化膜９からなるマスク３８を形成し、このマスク３８を用いて、シリコン基板１に酸素イオン３１を斜め回転イオン注入し、マスク３８の下部（この部分は、後の工程において、バーズビークが形成される部分である。）にまで広がる酸素注入層３４を、半導体基板１内部に形成する。

【０１０６】具体的には、酸素イオン３１の注入量は、例えば$1\times10^{15}cm^{-2}$以上を用い、注入エネルギーは例えば３０～１００ｋｅＶ程度を用い、注入角度は例えば３０～６０°程度を用いる。ここで、斜め回転イオン注入を用いることで、マスク３８の下部にまで酸素イオンが注入されることとなる。

【０１０７】次に、図１６（ｂ）に示すように、マスク３８を用いて、半導体基板１を熱酸化することにより、上記シリコン基板表面にＬＯＣＯＳ分離膜２０を形成する。ここで、斜め回転イオン注入により、マスク３８の下部にまで酸素イオンが注入されていたので、上記ＬＯＣＯＳ分離膜２０のバーズビーク付近での基準面４０より下の部分の厚さＴ２が、中央付近での上記厚さＴ１とほぼ等しくなるように、当該ＬＯＣＯＳ分離膜２０が形成されることとなる。

【０１０８】その後、上記マスク３８をエッチングにより除去し、注入量を低く抑えたイオン注入によりＰ型ウェル領域２を形成し、ＬＯＣＯＳ分離膜２０に囲まれた素子形成領域にＮ型拡散領域１８を形成することにより、図１５に示す半導体装置を得る。

【０１０９】ここで、バーズビーク付近でのＬＯＣＯＳ分離膜２０の基準面４０より下の部分の厚さＴ２が、中央付近での上記厚さＴ１とほぼ同じように形成されているので、上記ＬＯＣＯＳ分離膜２０に接する側の拡散領域の側面１９は、そのほとんどがＬＯＣＯＳ分離膜２０と接することとなる。

【０１１０】したがって、本発明の実施の形態６に示す半導体装置によれば、Ｎ型拡散領域１８とＰ型ウェル領域２の接触面積を低減することができ、そのため、接合容量を低減することが可能となる。

【０１１１】なお、本実施の形態６においては、ウェル領域２の導電型をＰ型に、拡散領域１８の導電型をＮ型としていたが、互いに、他の一方の導電型を有するものとしても良く、この場合においても、上記と同様の効果を有する。

【０１１２】実施の形態７．図１７は、本発明の実施の形態７を示す要部断面図であり、図１７において、１は

19

シリコン基板であり、２は不純物濃度の非常に低いＰ型ウェル領域、５はシリコン基板１表面に形成された素子分離層であるＬＯＣＯＳ分離膜である。１８はＬＯＣＯＳ分離膜５に囲まれたＮ型ＭＯＳトランジスタ形成領域４１中に形成されている不純物濃度の高いＮ型拡散領域であり、２１はＬＯＣＯＳ分離膜５の中央付近の下にのみ形成された、ウェル領域２に比べ高い不純物濃度を有するＰ型チャネルカット領域である。

【０１１３】図１７に示す半導体装置においては、接合容量を増加させないために、Ｎ型拡散領域１８の周囲のウェル領域２の不純物濃度を非常に低くしているが、一方において、ＬＯＣＯＳ分離膜５のパンチスルー効果による分離耐圧の劣化を防止するために、このＬＯＣＯＳ分離膜５の中央付近の下にのみ、ウェル領域２に比べ高い不純物濃度を有するＰ型チャネルカット領域２１を形成している。

【０１１４】図１７に示す半導体装置を得るため、図１８に示す製造方法を提案する。図１８にて示す半導体装置の製造方法においては、シリコン基板１の表面にＬＯＣＯＳ分離膜５を形成後、Ｐ型ウェル領域２を形成し、その後、ＬＯＣＯＳ分離膜５の中央付近に開口するレジストマスク２２を形成し、このマスク２２を用いたボロンイオン３２の注入を行うことで、ＬＯＣＯＳ分離膜５の中央付近の下にのみ、ウェル領域２のに比べ高い不純物濃度を有するＰ型チャネルカット領域２１を形成する。

【０１１５】しかし、この図１８にて示す半導体装置の製造方法では、チャネルカット領域２１の形成用のマスク２２を形成するための写真製版工程が必要となり、製造コストが上昇するという問題が発生する。

【０１１６】そこで、本実施の形態７においては、上記問題を解決するために、図１９に示す製造方法を用いて半導体装置を製造する。図１９（ａ）に示すように、まず、実施の形態２にて示した半導体装置の製造方法を用いて、ＬＯＣＯＳ分離膜５を半導体基板１の表面に形成する。ここで、このＬＯＣＯＳ分離膜５は、実施の形態２にて示したように、ＬＯＣＯＳ分離膜５内部の下面近傍に窒化酸化シリコン層１３を有している。その後、イオン注入により不純物濃度が非常に低いＰ型ウェル領域２をシリコン基板１に形成する。

【０１１７】次に、図１９（ｂ）に示すように、ボロンイオン３２ａを斜め回転イオン注入する。このとき、ボロンイオン３２ａの投影飛程は、シリコン基板１に対するより、窒化酸化シリコン層１３に対応する方が低い値を示すので、上記ＬＯＣＯＳ分離膜５内部の下面近傍に窒化酸化シリコン層１３が存在しているため、ＬＯＣＯＳ分離膜５の中央付近の下にのみ、ボロンの不純物濃度が、その周囲に比べて高くなる領域２３が形成される。なぜなら、その中央部分のみが左右からのチャネルカット注入イオン３２ａが足し会わされることとなるからである。

20

【０１１８】次に、図１９（ｃ）に示すように、アニール処理を行うことにより、高濃度の不純物領域２３から、不純物であるボロンを再拡散させ、ウェル領域２に比べ高い不純物濃度を有するＰ型チャネルカット領域２１を形成する。

【０１１９】その後、イオン注入により、ＬＯＣＯＳ分離膜５に囲まれたＮ型ＭＯＳトランジスタ形成領域４１にＮ型拡散領域１８を形成し、図１７に示す半導体装置を得る。

【０１２０】本発明の実施の形態７に示す半導体装置の製造方法においては、チャネルカット領域２１の形成用のマスクを形成するための写真製版工程が不要となり、製造コストが低減することができるという効果を有する。

【０１２１】実施の形態８．以下に、この発明の実施の形態８について図２０及び図２１に基づいて説明する。図２０は、本発明の実施の形態８を示す要部断面図であり、図２０において、１はシリコン基板であり、２ａは不純物濃度の非常に低いＮ型ウェル領域、５はシリコン基板１表面に形成された素子分離層であるＬＯＣＯＳ分離膜である。１８ａはＬＯＣＯＳ分離膜５に囲まれたＰ型ＭＯＳトランジスタ形成領域４２中に形成されている不純物濃度の高いＰ型拡散領域であり、２１ａはＬＯＣＯＳ分離膜５の中央付近の下にのみ形成された、ウェル領域２ａに比べ高い不純物濃度を有するＮ型チャネルカット領域である。

【０１２２】図２０に示す半導体装置においては、接合容量を増加させないために、Ｐ型拡散領域１８ａの周囲のウェル領域２ａの不純物濃度を非常に低くしているが、一方において、ＬＯＣＯＳ分離膜５のパンチスルー効果による分離耐圧の劣化を防止するために、このＬＯＣＯＳ分離膜５の中央付近の下にのみ、ウェル領域２ａに比べ高い不純物濃度を有するＮ型チャネルカット領域２１ａを形成している。

【０１２３】つぎに、このように構成された半導体装置の製造方法について図２１を用いて説明する。図２１は本実施の形態８を工程順に示す要部断面図である。

【０１２４】図２１（ａ）に示すように、まず、従来のＬＯＣＯＳ分離膜の製造方法を用いてＬＯＣＯＳ分離膜５を半導体基板１の表面に形成し、イオン注入により不純物濃度が非常に低いＮ型ウェル領域２ａをシリコン基板１に形成する。その後、リンイオン３３を斜め回転イオン注入する。このとき、リンイオン３３の投影飛程は、シリコン基板１に対するより、酸化シリコン層からなるＬＯＣＯＳ分離膜５に対応する方が低い値を示すので、ＬＯＣＯＳ分離膜５の中央付近の下にのみ、リンの不純物濃度が、その周囲に比べて高くなる領域２４が形成される。なぜなら、その中央部分のみが左右からのチャネルカット注入イオン３３が足し会わされることとな

るからである。

【０１２５】次に、図２１（ｂ）に示すように、アニール処理を行うことにより、高濃度の不純物領域２４から、不純物であるリンを再拡散させ、ウェル領域２ａに比べ高い不純物濃度を有するＮ型チャネルカット領域２１ａを形成する。

【０１２６】その後、イオン注入により、ＬＯＣＯＳ分離膜５に囲まれたＰ型ＭＯＳトランジスタ形成領域４２にＰ型拡散領域１８ａを形成し、図２０に示す半導体装置を得る。

【０１２７】本発明の実施の形態８に示す半導体装置の製造方法においては、チャネルカット領域２１ａの形成用のマスクを形成するための写真製版工程が不要となり、製造コストが低減することができるという効果を有する。

【０１２８】実施の形態９．以下に、この発明の実施の形態９である、上記図１７にて示した半導体装置の製造方法について、図２２に基づいて説明する。図２２は、本発明の実施の形態９を工程順に示す要部断面図である。

【０１２９】まず、図２２（ａ）に示すように、従来のＬＯＣＯＳ分離膜の製造方法により、多結晶シリコン膜８及びシリコン窒化膜９からなるマスク３９を用いて、シリコン基板１を熱酸化することにより、ＬＯＣＯＳ分離膜５をシリコン基板１表面に形成する。

【０１３０】次に、図２２（ｂ）に示すように、シリコン基板１上の全面にレジストを塗布し、エッチバックすることにより、マスク３９の側壁にサイドウォール２５を形成する。

【０１３１】ここで、次工程でのチャネルカット注入を、それぞれ異なる導電型を用いて行うことにより、Ｐ型領域とＮ型領域をそれぞれ指定する必要がある場合には、上記レジストのエッチバックを行う以前に、通常の写真製版技術を用いて、レジストをパターニングして、当該指定領域の一方の上部をレジストで覆っておけば良い。但し、この場合には、上記レジストのエッチバック時に、指定領域を覆っているレジストまでも除去してしまうことがないように、時間指定等の制限を設けた状態で上記エッチバックを行う。

【０１３２】次に、図２２（ｃ）に示すように、上記サイドウォール２５をマスクとして、ボロンイオン３２ｂを注入し、ＬＯＣＯＳ分離膜５の中央付近の下にのみＰ型チャネルカット領域２１を形成する。

【０１３３】次に、図２２（ｄ）に示すように、上記サイドウォール２５をウェット処理により除去する。

【０１３４】その後、イオン注入により、シリコン基板１にチャネルカット領域２１に比べ低い不純物濃度を有するウェル領域２を形成し、ＬＯＣＯＳ分離膜５に囲まれたＮ型ＭＯＳトランジスタ形成領域４１にＮ型拡散領域１８を形成して、図１７に示す半導体装置を得る。

【０１３５】上記のように形成された半導体装置においては、ＬＯＣＯＳ分離膜５の中央付近の下にのみ、ウェル領域２に比べ高い不純物濃度を有するＰ型チャネルカット領域２１を形成しているので、ＬＯＣＯＳ分離膜５のパンチスルー効果による分離耐圧の劣化を防止でき、しかも、Ｎ型拡散領域１８の周囲のウェル領域２の不純物濃度を非常に低くしているので、接合容量を増加させることはない。

【０１３６】又、本発明の実施の形態９に示す半導体装置の製造方法においては、チャネルカット領域２１の形成用のマスクであるサイドウォール２５を、改めてアライメントする必要がなく、自己整合的に、ＬＯＣＯＳ分離膜５の中央付近の下にのみＰ型チャネルカット領域２１を形成できるようにマスク２５を形成することが可能となる。

【０１３７】又、本発明の実施の形態９に示す半導体装置の製造方法においては、チャネルカット領域２１の形成のために、斜め回転イオン注入をする必要がなく、そのため、製造コストを低減できるという効果を有する。

【０１３８】しかも、ＬＯＣＯＳ分離膜５の形成後に、上記ボロンイオン３２ｂの注入を行っているので、ＬＯＣＯＳ分離膜５の形成前にボロンイオンの注入を行う場合に比べ、当該ＬＯＣＯＳ分離膜５の形成のための高温の熱処理工程における注入ボロン原子の再分布が起こらいという利点を有する。

【０１３９】なお、本実施の形態９においては、ウェル領域２及びチャネルカット領域２１の導電型をＰ型に、拡散領域１８の導電型をＮ型としていたが、互いに、他の一方の導電型を有するものとしても良く、この場合においても、上記と同様の効果を有する。

【０１４０】実施の形態１０．以下に、この発明の実施の形態１０である、上記図１７にて示した半導体装置の製造方法について、図２３に基づいて説明する。図２３は、本発明の実施の形態１０を工程順に示す要部断面図である。

【０１４１】まず、図２３（ａ）に示すように、表面にシリコン酸化膜７が形成されているシリコン基板１上に、多結晶シリコン膜８、シリコン窒化膜９及びレジストをこの順に積層して、通常の写真製版技術を用いてレジストをパターニングし、このパターニングされたレジストをマスクとして多結晶シリコン膜８及びシリコン窒化膜９のエッチングを行い、上記エッチングされた多結晶シリコン膜８及びシリコン窒化膜９からなるマスク３９を形成する。

【０１４２】次に、図２３（ｂ）に示すように、シリコン基板１上の全面にレジストを塗布し、エッチバックすることにより、マスク３９の側壁にサイドウォール２６を形成する。

【０１４３】ここで、次工程でのチャネルカット注入を、それぞれ異なる導電型を用いて行うことにより、Ｐ

型領域とＮ型領域をそれぞれ指定する必要がある場合には、上記レジストのエッチバックを行う以前に、通常の写真製版技術を用いて、レジストをパターニングして、当該指定領域の一方の上部をレジストで覆っておけば良い。但し、この場合には、上記レジストのエッチバック時に、指定領域を覆っているレジストまでも除去してしまうことがないように、時間指定等の制限を設けた状態で上記エッチバックを行う。

【０１４４】又、ここで、上記サイドウォール２６の材質として、上記レジストに代えて、ドライエッチングに対する選択比が多結晶シリコン膜８及びシリコン窒化膜９よりも高い材質を用いても良く、又、ウェット処理による除去が可能な材質を用いても良い。

【０１４５】次に、図２３（ｃ）に示すように、上記サイドウォール２６をマスクとして、ボロンイオン３２ｃを注入し、以降の工程において形成されるＬＯＣＯＳ分離膜５の中央付近の下にのみ位置するように、Ｐ型チャネルカット領域２１を形成する。

【０１４６】次に、図２３（ｄ）に示すように、上記サイドウォール２６をウェット処理により除去する。

【０１４７】次に、図２３（ｅ）に示すように、多結晶シリコン膜８及びシリコン窒化膜９からなるマスク３９を用いて、熱酸化することにより、シリコン基板１表面の上記Ｐ型チャネルカット領域２１直上に、ＬＯＣＯＳ分離膜５を形成する。

【０１４８】その後、イオン注入により、シリコン基板１にチャネルカット領域２１に比べ低い不純物濃度を有するウェル領域２を形成し、ＬＯＣＯＳ分離膜５に囲まれたＮ型ＭＯＳトランジスタ形成領域４１にＮ型拡散領域１８を形成して、図１７に示す半導体装置を得る。

【０１４９】上記のように形成された半導体装置においては、ＬＯＣＯＳ分離膜５の中央付近の下にのみ、ウェル領域２に比べ高い不純物濃度を有するＰ型チャネルカット領域２１を形成しているので、ＬＯＣＯＳ分離膜５のパンチスルー効果による分離耐圧の劣化を防止でき、しかも、Ｎ型拡散領域１８の周囲のウェル領域２の不純物濃度を非常に低くしているので、接合容量を増加させることはない。

【０１５０】又、本発明の実施の形態１０に示す半導体装置の製造方法においては、チャネルカット領域２１の形成用のマスクであるサイドウォール２６を、改めてアライメントする必要がなく、自己整合的に、ＬＯＣＯＳ分離膜５の中央付近の下にのみＰ型チャネルカット領域２１を形成できるようにマスク２６を形成することが可能となる。

【０１５１】又、本発明の実施の形態１０に示す半導体装置の製造方法においては、チャネルカット領域２１の形成のために、斜め回転イオン注入をする必要がなく、そのため、製造コストを低減できるという効果を有する。

【０１５２】しかも、ＬＯＣＯＳ分離膜５の形成のための熱酸化を行う前に、上記ボロンイオン３２ｃの注入を行っているので、ＬＯＣＯＳ分離膜５の形成後にボロンイオンの注入を行う場合に比べて、高エネルギーのボロンイオン注入装置を必要とせず、半導体装置の製造コストを全体として低減することが可能となる。

【０１５３】なお、本実施の形態１０においては、ウェル領域２及びチャネルカット領域２１の導電型をＰ型に、拡散領域１８の導電型をＮ型としていたが、互いに、他の一方の導電型を有するものとしても良く、この場合においても、上記と同様の効果を有する。

【０１５４】

【発明の効果】この発明に係る半導体装置は、シリコン基板の表面上に形成されたマスクを用いた当該シリコン基板の酸化により、上記シリコン基板表面に形成された素子分離層と、上記マスクを用いた上記シリコン基板への窒素のイオン注入により、上記素子分離層の下面近傍に形成された窒素含有層とを設けたので、チャネルカットのイオン注入量を、予め上記素子分離層への不純物イオンの吸い出し量を加えた分までイオン注入する必要がなく、そのため、ウェル中の不純物を全体として削減することができ、よって、当該半導体装置における接合容量を低減することができるという効果を有する。

【０１５５】又、半導体基板表面に形成された素子分離層を備え、上記半導体基板表面の内、当該素子分離層が形成されている部分の近傍であり、かつ上記素子分離層が形成されていない部分を、当該素子分離層内部にまで延長した面を基準面として、上記素子分離層が、上記基準面に対する垂直断面における幅が異なる複数の領域を有するとともに、その幅に関係なく厚さがほぼ一定であるので、チャネルカット領域を形成するためのイオン注入の、注入エネルギーの最適化が容易であり、そのため、当該半導体装置における接合容量を低減することができるという効果を有する。

【０１５６】又、半導体基板表面に形成された素子分離層を備え、上記半導体基板表面の内、当該素子分離層が形成されている部分の近傍であり、かつ上記素子分離層が形成されていない部分を、当該素子分離層内部にまで延長した面を基準面として、上記素子分離層が、上記基準面に対する垂直断面における幅が異なる複数の領域を有するとともに、その幅に関係なく上記基準面より上の部分の厚さがほぼ一定であるので、チャネルカット領域を形成するためのイオン注入の、注入エネルギーの最適化が容易であり、そのため、当該半導体装置における接合容量を低減することができるという効果を有し、さらに、上記素子分離層上に形成される配線の寸法のばらつきを少なくできるという効果も有する。

【０１５７】又、半導体基板の表面に形成された素子分離層と、上記半導体基板の素子分離層が形成されている面の、上記素子分離層に囲まれた領域に形成されるとと

もに、側面が上記素子分離層に接している拡散領域とを備え、上記半導体基板表面の内、当該素子分離層が形成されている部分の近傍であり、かつ上記素子分離層が形成されていない部分を、当該素子分離層内部にまで延長した面を基準面として、上記素子分離層は、この基準面に対する垂直断面において、当該垂直断面おける上記基準面より下の部分の厚さがほぼ一定であり、上記拡散領域は、上記素子分離層に接している側面のほとんどが当該素子分離層に接しているので、上記拡散領域の側面における、当該拡散領域とウェルとの接触面積を低減することができ、そのため、当該半導体装置における接合容量を低減することができるという効果を有する。

【０１５８】この発明に係る半導体装置の製造方法は、表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜、シリコン窒化膜及びレジストをこの順に積層して、マスクを形成する工程と、上記マスクを用いて、上記シリコン基板に窒素をイオン注入する工程と、上記マスクの一部であるレジストを除去する工程と、上記シリコン基板を上記レジストを除去したマスクを用いて熱酸化する工程とを具備するので、窒素をイオン注入するための写真製版工程をあらためて設ける必要がなく、そのため、工程数を削減できるという効果を有し、さらに、高エネルギーのイオン注入機が不要であるので、製造コストを低く抑えることが可能であるという効果も有する。

【０１５９】又、表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜及びシリコン窒化膜をこの順に積層して、マスクを形成する工程と、上記シリコン基板を上記マスクを用いて熱酸化する工程と、上記マスクを用いて、上記シリコン基板に窒素をイオン注入する工程とを具備するので、窒素をイオン注入するための写真製版工程をあらためて設ける必要がなく、そのため、工程数を削減できるという効果を有し、さらに、上記熱処理による窒素の拡散が生じず、窒化シリコン層又は窒化酸化シリコン層の膜厚の制御、及び、上記窒化シリコン層又は窒化酸化シリコン層中の窒素の含有量及び深さの制御が容易であるという効果を有する。

【０１６０】又、半導体基板の表面上にマスクを形成する工程と、上記半導体基板を上記マスクを用いて熱酸化することにより、素子分離層を形成する工程と、上記マスクを用いて、上記素子分離層をドライエッチングする工程とを具備するので、上記素子分離層を形成するマスクの開口幅が異なる場合にも、そのマスクの開口幅の違いによるマイクロローデイング効果の相違により、各素子分離層に対するドライエッチングの速度が異なるので、当該素子分離層を上記マスクの開口幅に関係なくほぼ一定の厚さに形成することができるという効果を有する。

【０１６１】又、半導体基板の表面上にマスクを形成する工程と、上記半導体基板を上記マスクを用いて熱酸化

することにより、素子分離層を形成する工程と、上記半導体基板上に絶縁膜を形成する工程と、上記絶縁膜を平坦化する工程と、上記マスクの上端の一部が露出するまで、上記平坦化した絶縁膜を除去する工程と、上記マスクを除去する工程とを具備するので、上記素子分離層を形成するマスクの開口幅が異なる場合にも、上記マスクの開口幅に関係なく、上記半導体基板表面の内、当該素子分離層が形成されている部分の近傍であり、かつ上記素子分離層が形成されていない部分を、当該素子分離層内部にまで延長した面を基準面として、当該素子分離層の上記基準面より上の部分をほぼ一定の厚さに形成することができるという効果を有する。

【０１６２】又、表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜及びシリコン窒化膜をこの順に積層して、マスクを形成する工程と、上記マスクを用いて、上記シリコン基板に酸素を斜め回転イオン注入する工程と、上記シリコン基板を上記マスクを用いて熱酸化する工程とを具備するので、上記半導体基板表面の内、上記熱酸化により形成される素子分離層の近傍であり、かつ、この素子分離層が形成ない部分を、当該素子分離層内部にまで延長した面を基準面として、上記基準面に対する当該素子分離層の垂直断面において、当該垂直断面における上記基準面より下の部分をほぼ一定の厚さに形成することができるという効果を有する。

【０１６３】又、シリコン基板の一主面に素子分離層を形成する工程と、上記シリコン基板の一主面にリンを斜め回転イオン注入することにより、チャネルカット領域を形成する工程とを具備するので、上記素子分離領域の直下で、かつ、当該素子分離領域の中央付近のリンの濃度を高くすることができ、そのため、接合容量の低い半導体装置を形成することができるという効果を有し、さらに、上記リンのイオン注入のために、あらためてマスクを形成する必要がなく、製造工程の簡略化が図れるという効果を有する。

【０１６４】又、シリコン基板の一主面に、窒化酸化シリコン層を有する素子分離層を形成する工程と、上記シリコン基板の一主面にボロンを斜め回転イオン注入することにより、チャネルカット領域を形成する工程とを具備するので、上記素子分離領域の直下で、かつ、当該素子分離領域の中央付近のボロンの濃度を高くすることができ、そのため、接合容量の低い半導体装置を形成することができるという効果を有し、さらに、上記ボロンのイオン注入のために、あらためてマスクを形成する必要がなく、製造工程の簡略化が図れるという効果を有する。

【０１６５】又、表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜及びシリコン窒化膜をこの順に積層して、マスクを形成する工程と、上記シリコン基板を上記マスクを用いて熱酸化する工程と、上記マスク側面にレジストからなるサイドウォールを形成

する工程と、上記サイドウォールをマスクとして、上記シリコン基板内部に不純物をイオン注入する工程と、上記サイドウォールをエッチングにより除去する工程とを具備するので、上記素子分離領域の直下の当該素子分離領域の中央付近に位置するチャネルカット領域の、不純物濃度を高くすることができ、そのため、接合容量の低い半導体装置を形成することができるという効果を有する。

【０１６６】又、表面にシリコン酸化膜が形成されたシリコン基板上に、多結晶シリコン膜及びシリコン窒化膜をこの順に積層して、マスクを形成する工程と、上記マスクの側面にレジストからなるサイドウォールを形成する工程と、上記サイドウォールをマスクとして、上記シリコン基板内部に不純物をイオン注入する工程と、上記サイドウォールをエッチングにより除去する工程と、上記多結晶シリコン膜及びシリコン窒化膜からなるマスクを用いて、上記シリコン基板を熱酸化する工程とを具備するので、上記素子分離領域の直下の当該素子分離領域の中央付近に位置するチャネルカット領域の、不純物濃度を高くすることができ、そのため、接合容量の低い半導体装置を形成することができるという効果を有する。

【図面の簡単な説明】

【図１】　この発明の実施の形態１を示す要部平面図。

【図２】　この発明の実施の形態１を工程順に示す要部断面図。

【図３】　この発明の実施の形態１を工程順に示す要部断面図。

【図４】　この発明の実施の形態２を示す要部平面図。

【図５】　この発明の実施の形態３を示す要部平面図。

【図６】　この発明の実施の形態３を工程順に示す要部断面図。

【図７】　従来の半導体装置示す要部断面図。

【図８】　この発明の実施の形態４を示す要部断面図。

【図９】　この発明の実施の形態４を工程順に示す要部断面図。

【図１０】　この発明の実施の形態４を示す要部断面図。

【図１１】　この発明の実施の形態４を工程順に示す要部断面図。

【図１２】　この発明の実施の形態５を示す要部断面図。

【図１３】　この発明の実施の形態５を工程順に示す要

部断面図。

【図１４】　従来の半導体装置示す要部断面図。

【図１５】　この発明の実施の形態６を示す要部断面図。

【図１６】　この発明の実施の形態６を工程順に示す要部断面図。

【図１７】　この発明の実施の形態７を示す要部断面図。

【図１８】　図１７に示す半導体装置の製造方法の１提案例を示す要部断面図。

【図１９】　この発明の実施の形態７を工程順に示す要部断面図。

【図２０】　この発明の実施の形態８を示す要部断面図。

【図２１】　この発明の実施の形態８を工程順に示す要部断面図。

【図２２】　この発明の実施の形態９を工程順に示す要部断面図。

【図２３】　この発明の実施の形態１０を工程順に示す要部断面図。

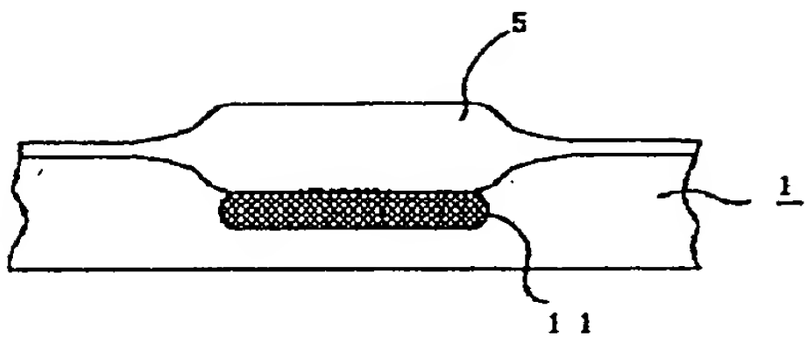
【図２４】　従来の半導体装置示す要部断面図。

【図２５】　従来の半導体装置の製造方法を工程順に示す要部断面図。

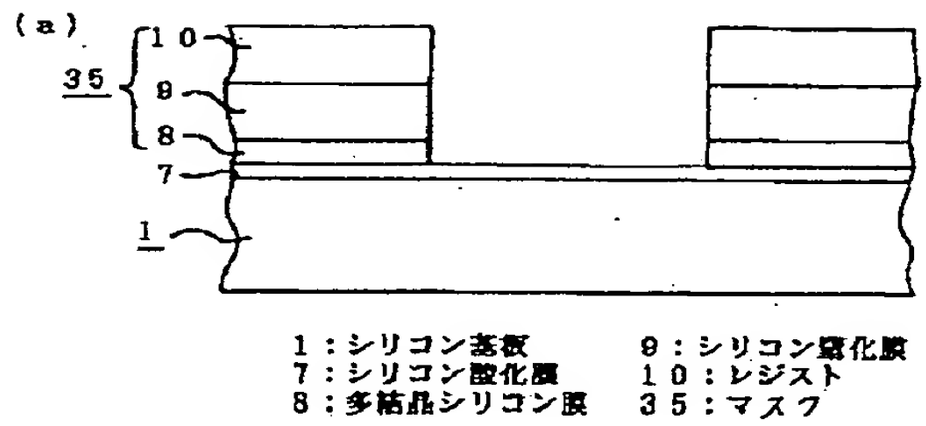
【符号の説明】

１　半導体基板（シリコン基板）、　５　素子分離層、５ａ、５ｂ、５ｃ、５ｄ、５ｅ、５ｆ、５ｇ、５ｈ　素子分離層の一領域、７　シリコン酸化膜、　８　多結晶シリコン、　９　シリコン窒化膜、１０　レジスト、１１　窒素含有層（窒化シリコン層）、１３　窒素含有層（窒化酸化シリコン層）、　１７　絶縁膜、１８　拡散領域、　１９　拡散領域の側面、　２０　素子分離層、２１、２１ａ　チャネルカット領域、　２３　注入されたボロン、２４　注入されたリン、　２５、２６　サイドウォール、３０ａ、３０ｂ、３０ｃ　窒素イオン、　３１　酸素イオン、３２ａ　ボロンイオン、３２ｂ、３２ｃ　不純物イオン、３３　リンイオン、３５、３６、３７、３８、３９　マスク、４０　基準面、Ｗ１、Ｗ２　素子分離層の一領域の幅、ｘ１、ｘ２　素子分離層の一領域の基準面より上の部分の厚さ、ｚ１、ｚ２　素子分離層の一領域の厚さ、ｔ１、ｔ２　素子分離層の一領域の基準面より上の部分の厚さ、Ｔ１、Ｔ２　素子分離層の基準面より下の部分の厚さ。

【図１】



【図２】

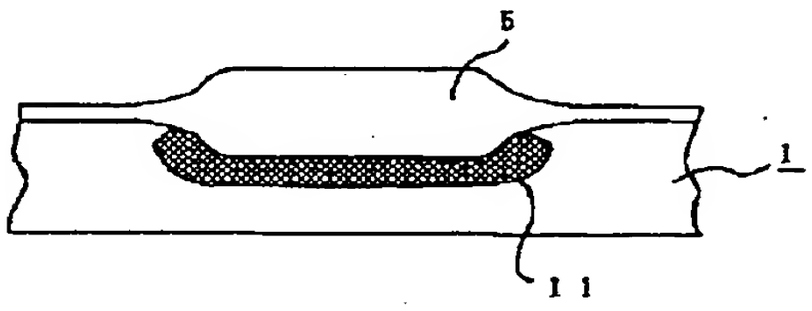


1：シリコン基板　　9：シリコン窒化膜
7：シリコン酸化膜　　10：レジスト
8：多結晶シリコン膜　　35：マスク

12a：窒素注入層　　30a：窒素イオン

5：LOCOS分離膜
11：窒化シリコン層

【図５】



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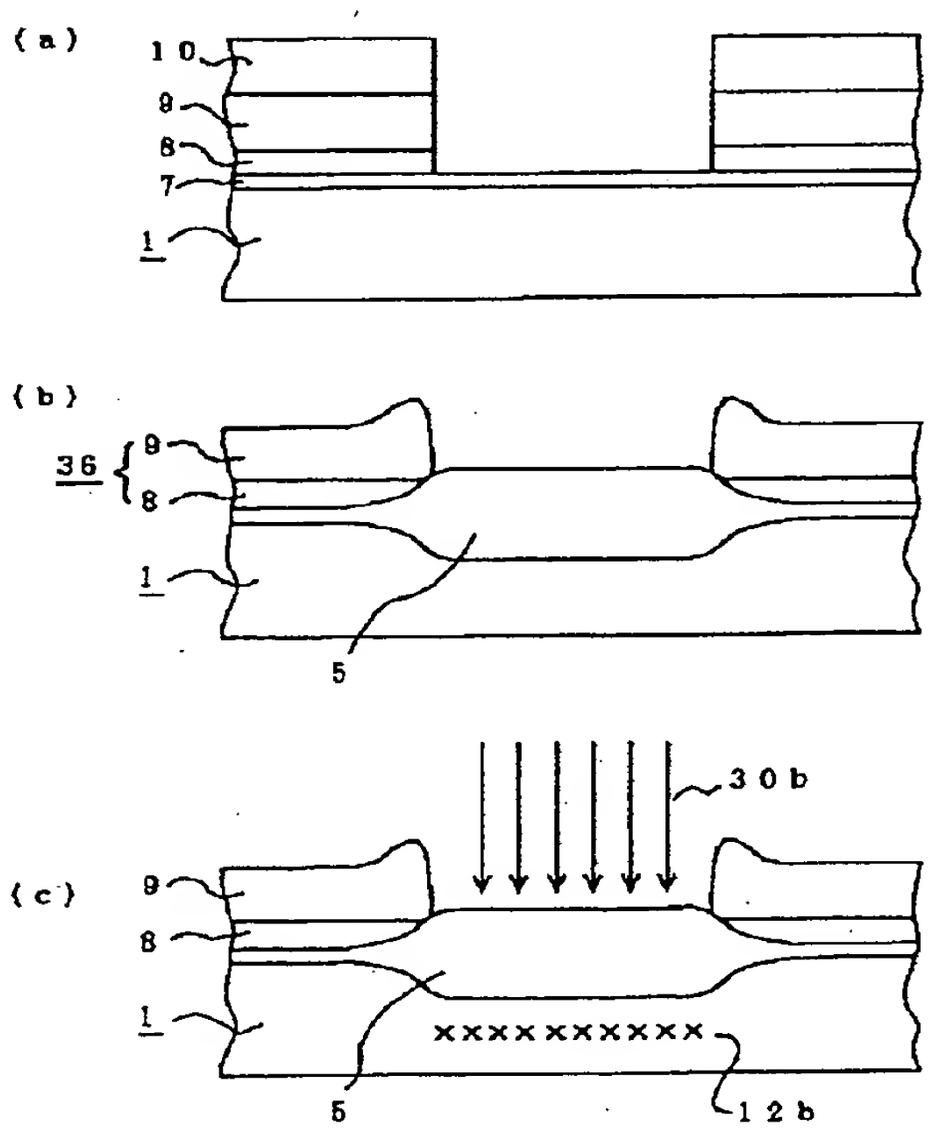

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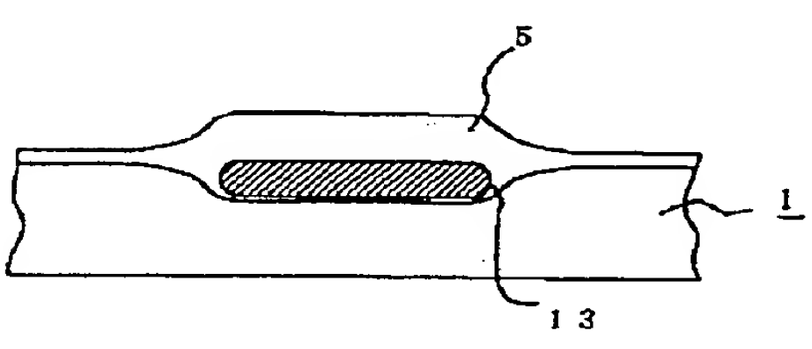

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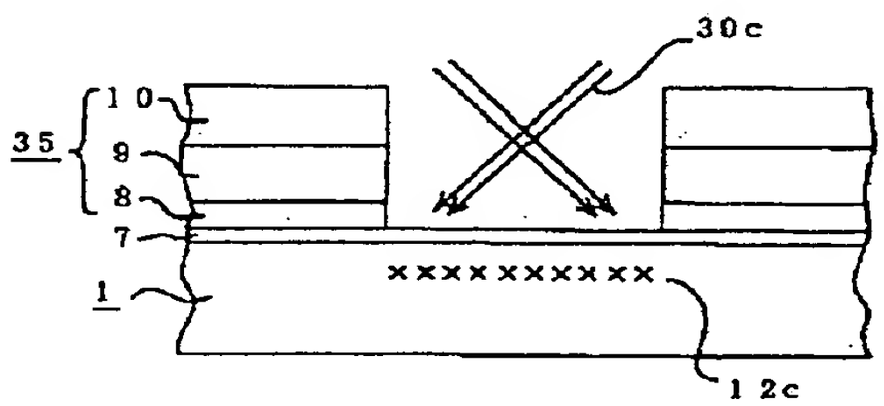

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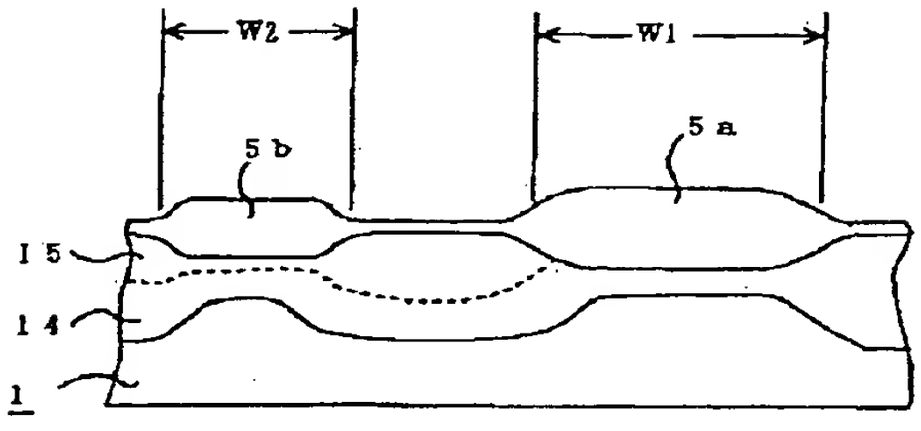

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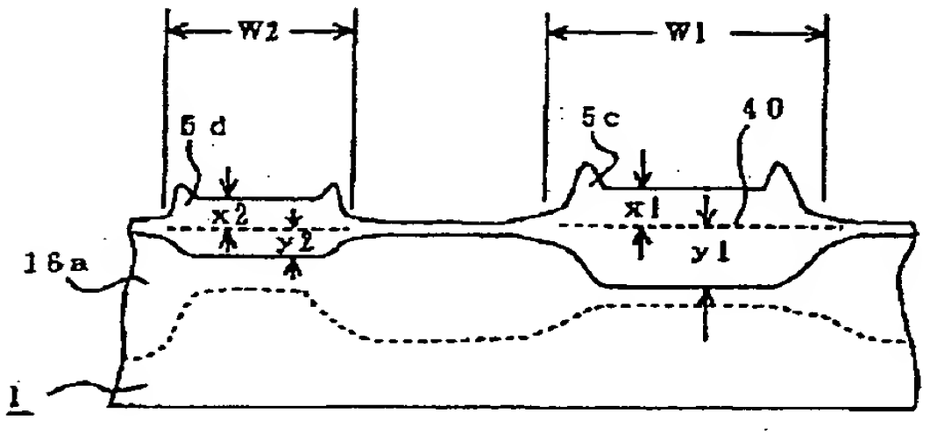

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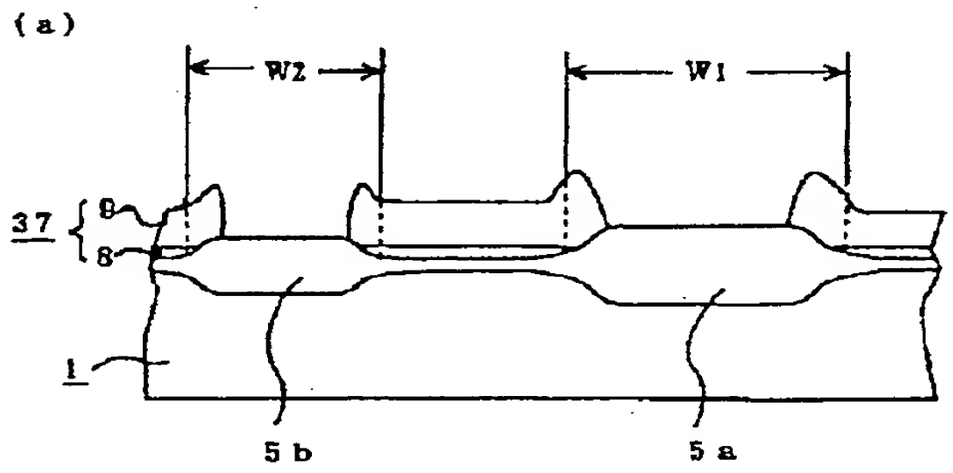

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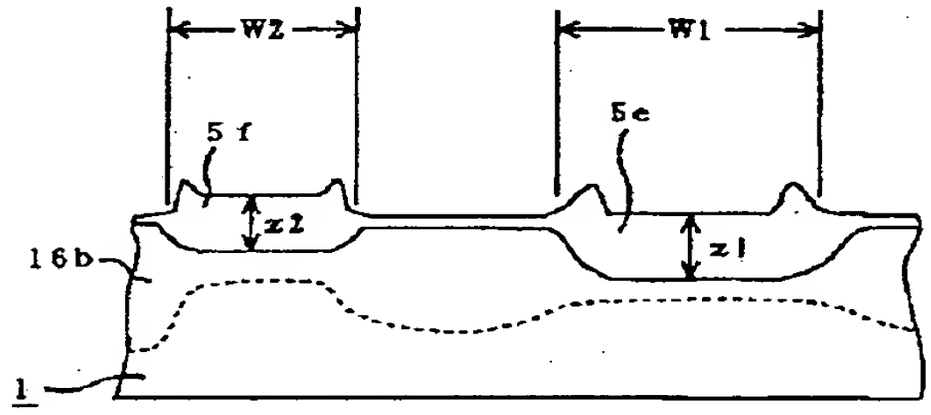
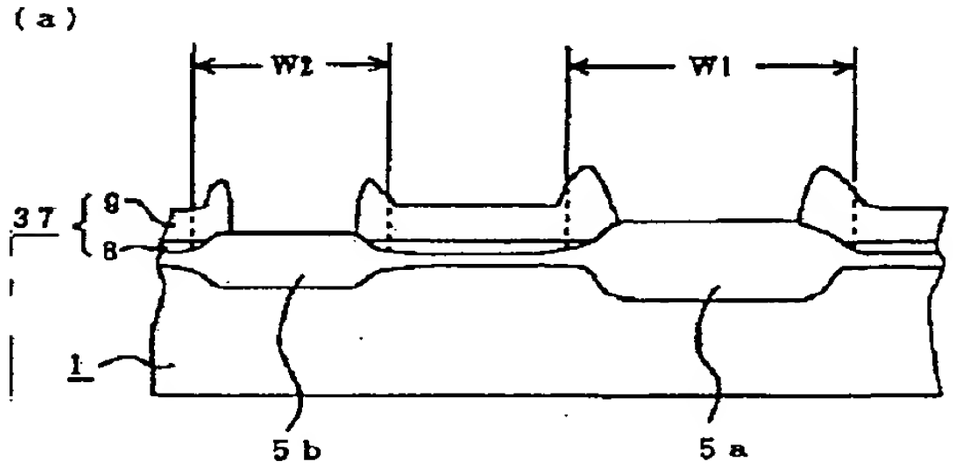


【図１１】



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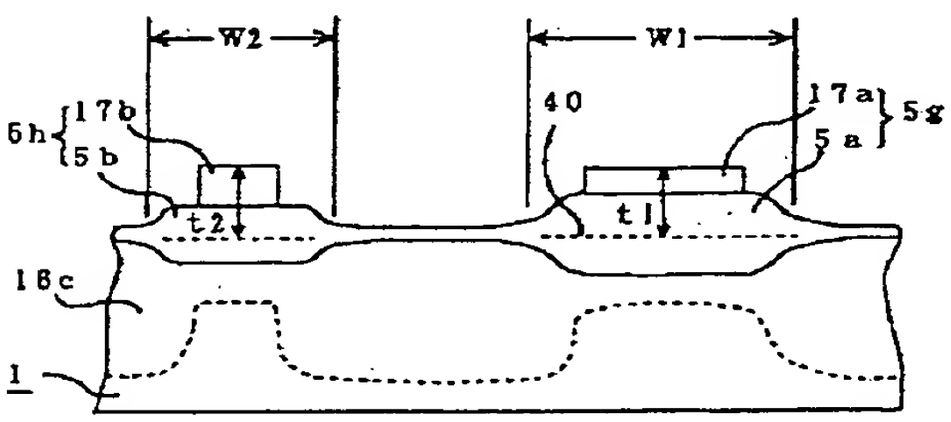

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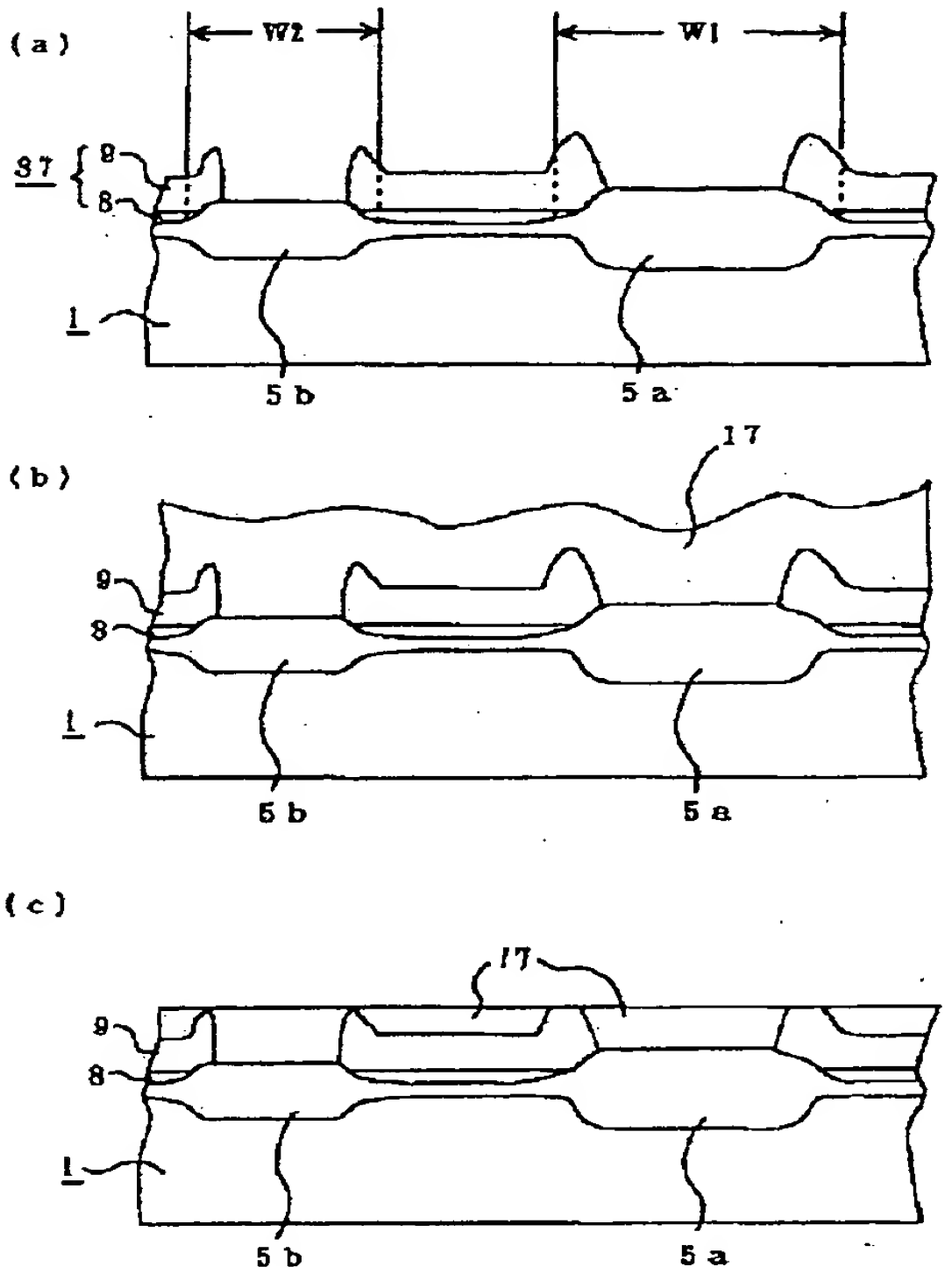

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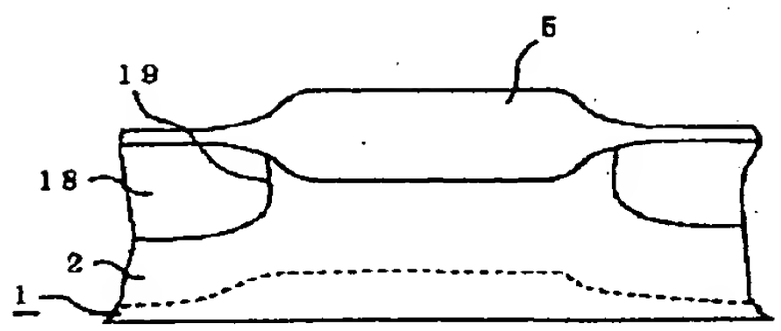

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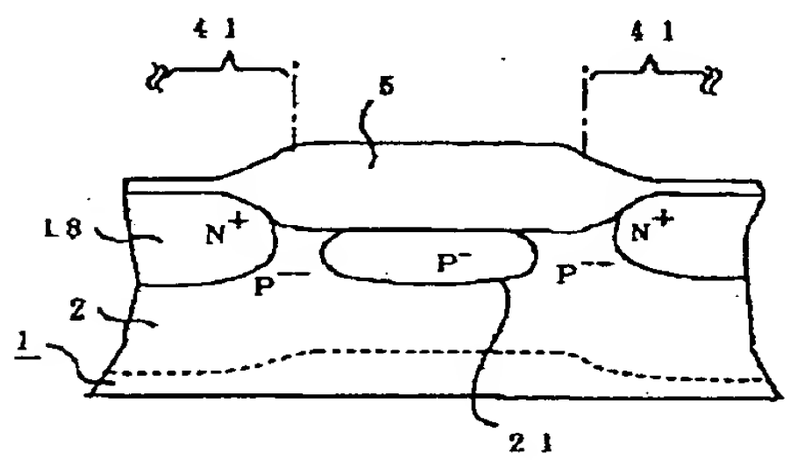

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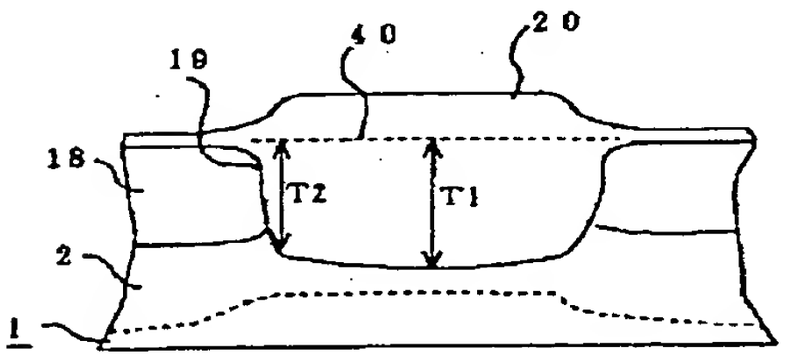

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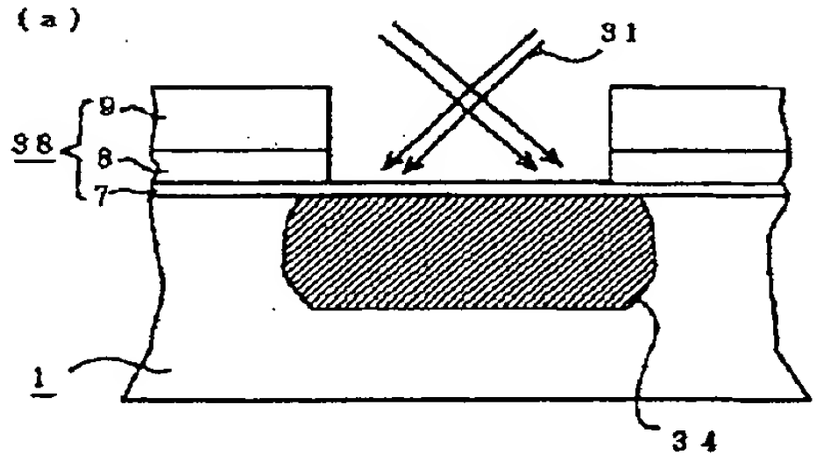

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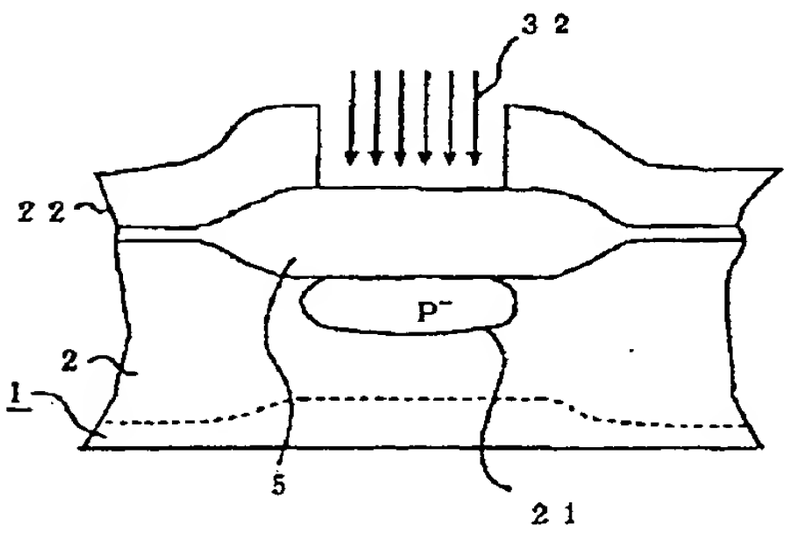

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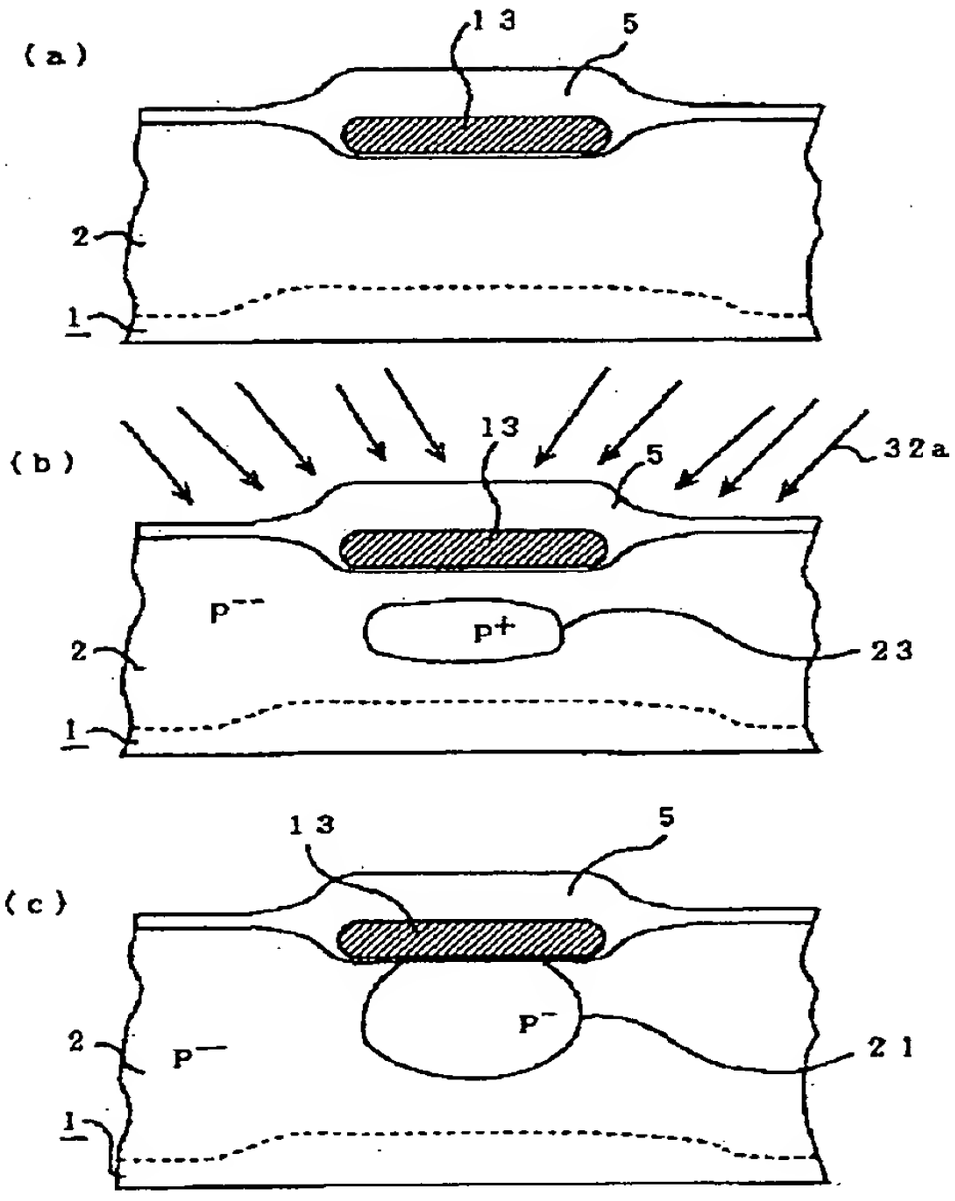

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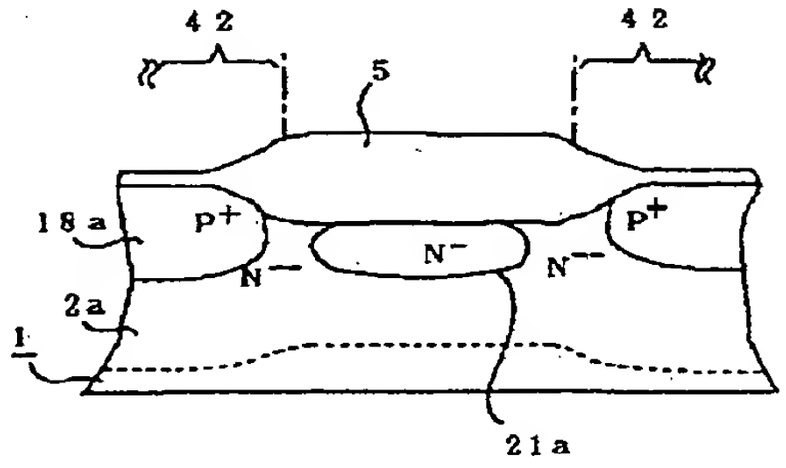
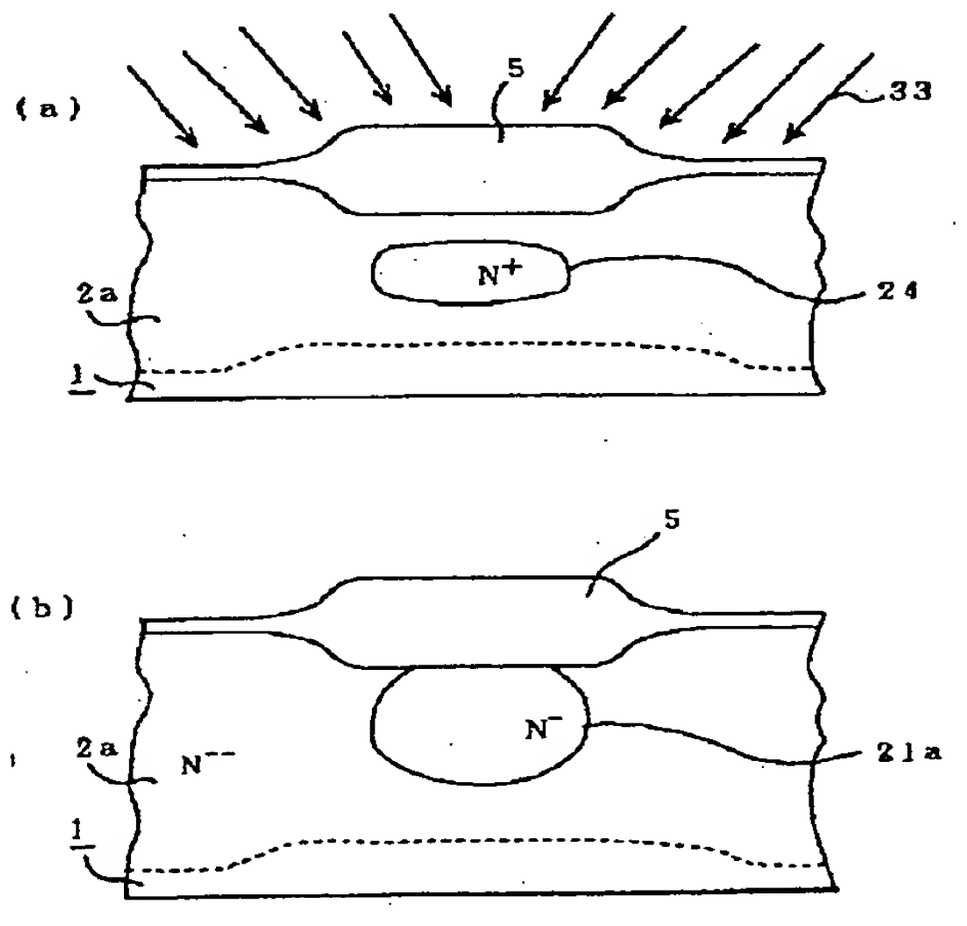


【図２１】



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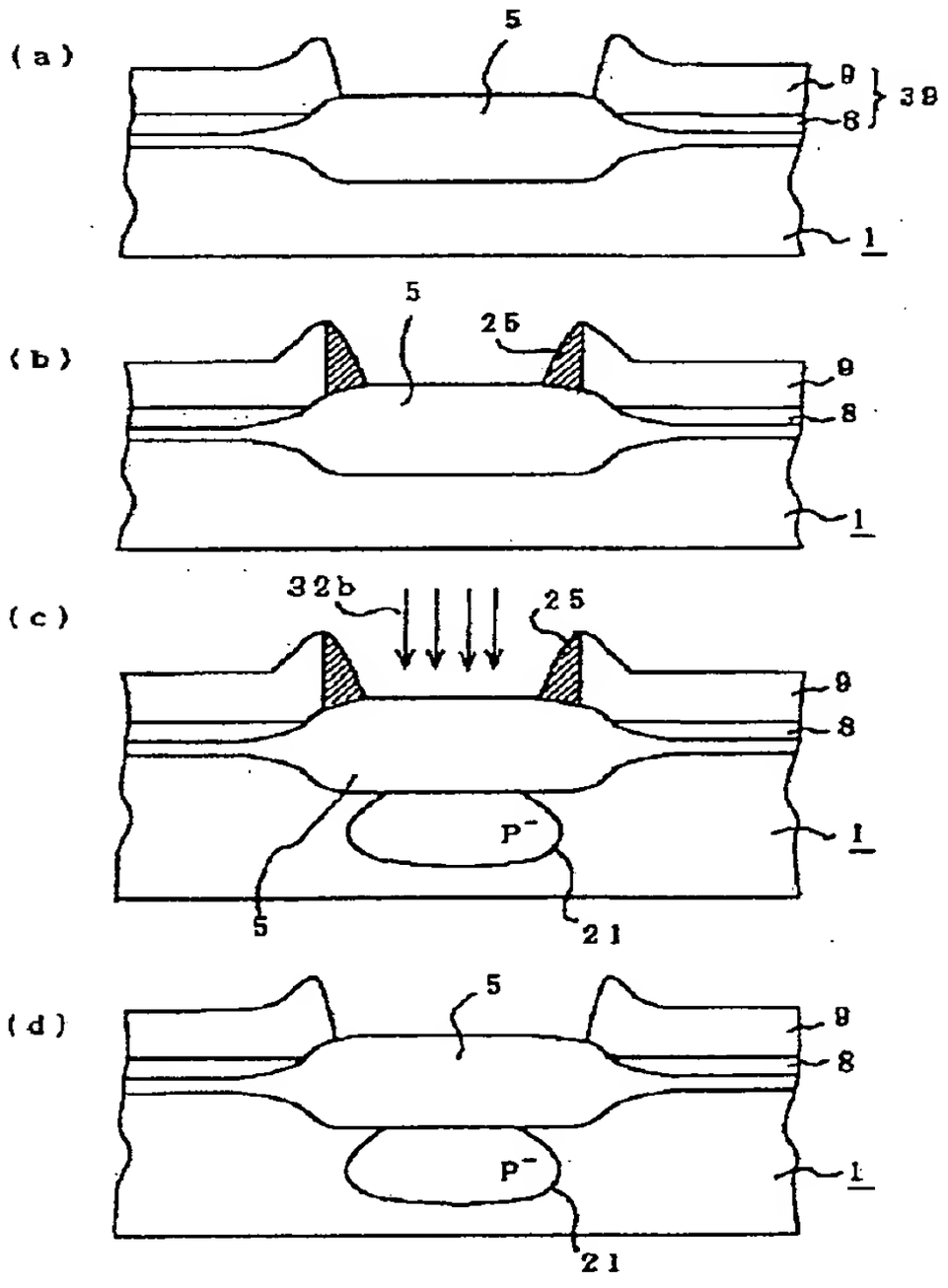

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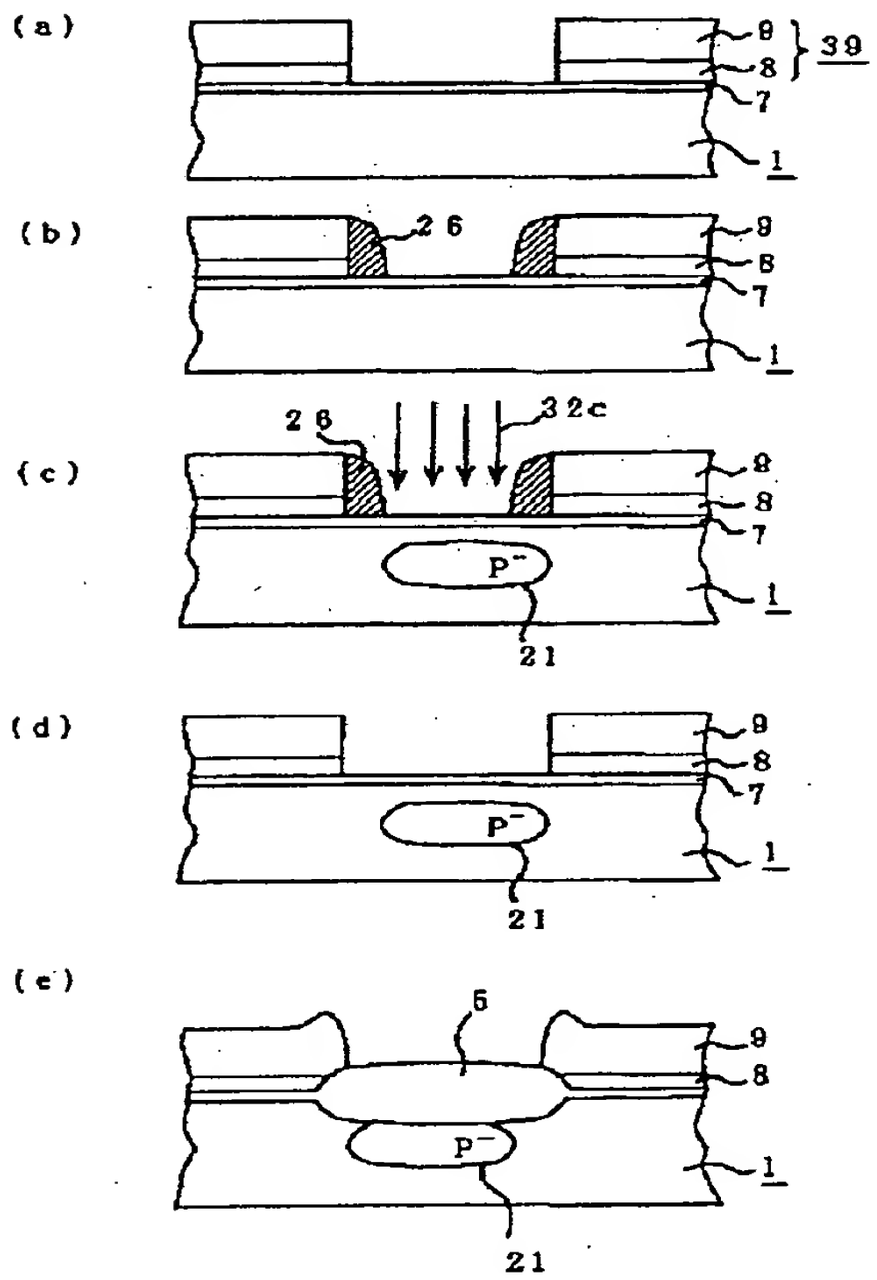

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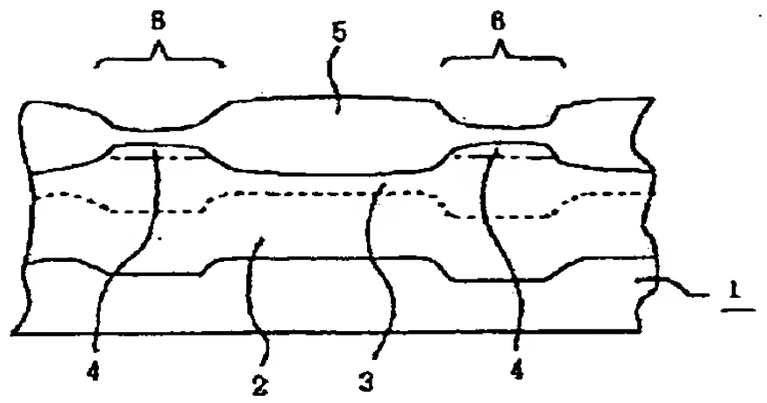

1：シリコン基板
2：ウェル領域
3：チャネルカット領域
4：チャネルドープ領域
5：分離酸化膜
6：素子形成領域

【図２５】